AMIETE – CS/IT (NEW SCHEME) – Code: AC58/AT58

Subject: COMPUTER ORGANIZATION

Time: 3 Hours **JUNE 2009** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The number 100110_2 is numerically equivalent to

(A) 26_{10} **(B)** 36_{10}
(C) 46_8 **(D)** $2A2_{16}$

b. The basic performance equation for a computer is

(A) $T = \frac{N \times S}{R}$ **(B)** $T = \frac{N \times R}{S}$
(C) $T = \frac{S \times R}{N}$ **(D)** $N = \frac{S \times R}{T}$

c. In a digital computer binary subtraction is performed,

(A) In the same way as we perform subtraction in decimal number system.
(B) Using 2's complement method.
(C) Using 9's complement method.
(D) Using 10's complement method.

d. The maximum positive and negative numbers which can be represented in 2's complement from using n bits are

(A) $+(2^{n-1}-1), -(2^{n-1}-1)$ **(B)** $+(2^{n-1}-1), -2^{n-1}$
(C) $2^{n-1}, -2^{n-1}$ **(D)** $2^{n-1}, -(2^{n-1}+1)$

e. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600 respectively. What is the effective address of the memory operand for the following instructions (i) Load 20(R1), R5 (ii) Subtract R1, R5

(A) 1220 and 5830 **(B)** 5830 and 4599
(C) 1200 and 4599 **(D)** 1220 and 1200

f. The first byte of a 3 byte instruction will always have

(A) The address of memory
(B) An operand or address associated code
(C) opcode
(D) Anyone of the above.

g. A memory has 16 bit address bus. The number of locations in the memory are

(A) 16 **(B)** 32
(C) 1024 **(D)** 65536

h. 4 memory chips of 16×4 size have their address buses connected together. This system will be of size
(A) 64×4 **(B)** 16×16
(C) 32×8 **(D)** 256×1

i. 16 bytes are pulled from stack having top of stack address as 00CDH. What will be the new top of the stack.
(A) 00BDH **(B)** 00ADH
(C) 00DDH **(D)** 10CDH

j. The power consumption of a dynamic RAM is
(A) more than that of static RAM **(B)** double that of static RAM
(C) 5 times that of static RAM **(D)** $1/5$ of that of static RAM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Consider the memory system of a computer storing the following data:

Address in Hex	Data Stored (Binary)
2000	00111000
2001	00110100
2002	00110010
2003	00111001

Interpret the storage as numbers in
(i) Big Indian storage of 2 hex words of 4 digits each.
(ii) Big Indian storage of 2 BCD words of 4 digits each
(iii) Little Indian storage in ASCII of 4 digit signed hex words.
(iv) Little Indian storage in ASCII of 4 digit BCD word. **($4 \times 2\frac{1}{2} = 10$)**

b. Write a program that can evaluate the expression $A \times B + C \times D$ in a single accumulator processor. Assume that the processor has load, store, multiply and add instructions and that all values fit in the accumulator. **(6)**

Q.3 a. Register R5 is used in a program to point to the top of a stack. Write a sequence of instructions using index, Autoincrement, Autodecrement addressing modes to perform each of the following tasks:
(i) Pop the top 2 items off the stack, Add them, and then Push the result onto the stack.
(ii) Copy the fifth item from the top into register R_3.
(iii) Remove the top ten items from the stack. **($3 \times 3 = 9$)**

b. Explain any 4 logical instructions with examples for each. **(7)**

Q.4 a. Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line? **(8)**

b. What is the difference between a subroutine and ISR? Explain with example. **(4+4)**

Q.5 a. Why is bus arbitration required? Explain with block diagram bus arbitration using daisy chain? **(8)**

b. With a block diagram explain how a keyboard is connected to a processor. **(8)**

Q.6 a. Give a block diagram for $8M \times 32$ memory using $512K \times 8$ memory chips and explain. **(4+4)**

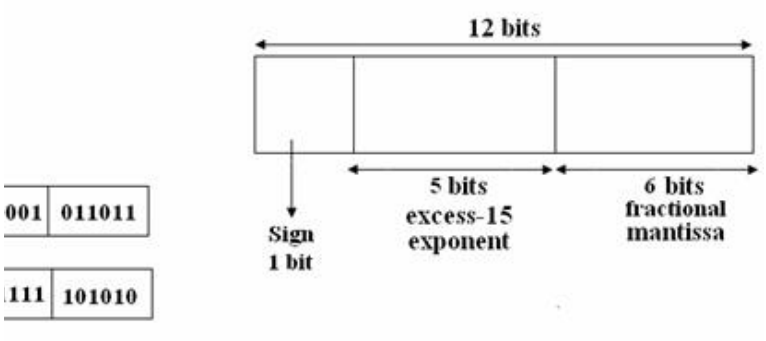
b. A block set associate cache consists of a total 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each consisting of 128 words.
(i) How many bits are there in the main memory address? **(4)**
(ii) How many bits are there in each of TAG, SET and WORD fields? **(4)**

Q.7 a. How many logic gates are needed to build the 4 bit carry look ahead Adder? Use the result of above to calculate how many logic gates are needed to build the 16 bit carry look ahead Adder. **(4+4)**

b. How virtual memory address translation is done? Explain with the help of a diagram. Compare cache techniques and virtual memory techniques. **(6+2)**

Q.8 a. Multiply the pairs of signed 2's complement numbers using Booth's algorithm A = 110011 (multiplicand), B = 101100 (multiplier) **(8)**

b. Perform addition on the following numbers considering the floating-point numbers represented in a 12-bit format as shown in the figure. **(8)**



Q.9 a. Write brief note on vertical and horizontal organizations. Which is more useful and where? **(6)**

b. Write the sequence of control steps required for single bus organisation for the instruction:
Add the contents of memory location NUM to register R1.
Assume that each instruction consists of two words. The first word specifies the operation and the addressing mode, the second word contains the number NUM. **(10)**