Reg. No. _____

Karunya University

(Karunya Institute of Technology and Sciences)

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November/December 2010

Subject Title : DIGITAL ELECTRONICS **Time : 3 hours**

Subject Code: EC209 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. Write the decimal number -39 as an 8 bit number in sign magnitude form.
2. Express the Boolean expression Y = AB + B(CD + EF) in SOP form.
3. What is the basic function of a comparator?
4. Assign the proper even parity bit for the code 10001010 1.
5. What is an edge triggered flip-flop?
6. What is a register?
7. Define state diagram.
8. Define execution table.
9. What is the bit capacity of a memory that can store 256 bytes of data?
10. What is fan out of a gate?

PART – B (5 x 3 = 15 MARKS)

11. Use the Karnaugh map to minimize the following expression.
$Y = A\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}\overline{B}CD + A\overline{B}CD + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D} + \overline{A}\overline{B}C\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$
12. Draw the logic diagram of a Binary to gray code converters using EX-OR gates.
13. Draw the block diagram and truth table of a 2 bit asynchronous binary counter.
14. Draw the state diagram of a D flip flop.
15. Mention the types of ROM.

PART – C (5 x 15 = 75 MARKS)

16. a. Perform the following operations: (8)
    i. Convert 100110011010 to octal.
    ii. Subtract $(84)_{16}$ - $(2A)_{16}$
    iii. Convert decimal 35 to BCD.
    iv. Convert binary 10110 to Gray code.

    b. State and prove the DeMorgan's theorems. (7)

(OR)

17. a. Explain with examples the 1's complement and 2's complement method of representing signed numbers. (8)

    b. Use Karnaugh map to simplify the following Boolean expression. (7)
    $Y = \Sigma(1, 2, 4, 6, 7)$

18. a. Implement the Boolean expression ABC + DE using NAND logic gates only. (7)

    b. What is a multiplexer? Describe with logic diagram a 4 x 1 multiplexer. (8)

(OR)

19. a. Explain the function of a full adder. (7)

    b. What is a parallel binary adder? Explain how it can be implemented using full adders. (8)

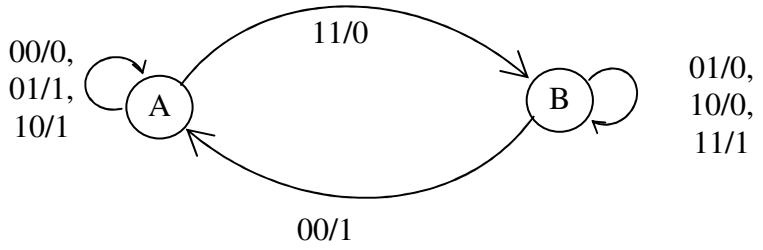
[P.T.O]

20. a. Describe the basic function of a SR and JK edge triggered flip flops with logic diagrams and truth table. (8)
    b. Implement a asynchronous counter using JK flip flops having a modulus of 12 counting from 0000 to 1011. (7)

(OR)

21. a. Design a synchronous counter which has the count sequence 001, 010, 101, and 111 using JK flip flops.

22. a. List the main steps involved in synthesis of synchronous sequential circuits. (5)
    b. Synthesize a serial binary adder whose state diagram is as follows. (10)



(OR)

23. A long sequence of pulses enter a 2 input 2 output synchronous sequential circuit which produces and output $Z = 1$ whenever the sequence 1111 occurs (overlapping sequences are accepted). Design the circuit.

24. Describe the basic PAL operation and how SOP expressions can be implemented in it.

(OR)

25. a. What are the voltage levels of TTL and CMOS logic?
    b. Explain the operation of a TTL and CMOS inverter circuit.