Reg. No. _____

Karunya University

(Karunya Institute of Technology and Sciences)

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – April/May 2011

Subject Title : DIGITAL ELECTRONICS **Time : 3 hours**

Subject Code: EC209 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. Show that the excess-3 code is self-complementing.
2. Find the complement of x + yz.
3. Mention the difference between a DEMUX and a MUX
4. Draw the logic diagram and truth table for a half subtractor.
5. Give the excitation table of J-K flip flop.
6. If a serial-in-serial-out shift register has N stages and if the clock frequency is f, what will be the time delay between input and output?
7. Define Flow table.
8. What is State Assignment?
9. What is non- volatile memory?
10. What is Configurable Logic Block?

PART – B (5 x 3 = 15 MARKS)

11. Express x + yz as the sum of min-terms.
12. Realize XOR function using only NAND gates
13. Draw the circuit diagram of a basic ring counter.
14. What is the difference between synchronous and asynchronous sequential logic circuits?
15. What is a PLA? Describe its uses.

PART – C (5 x 15 = 75 MARKS)

16. Simplify the following function by using tabulation method
    F= Σm (0, 2,3,6,7,8,10,12,13)

(OR)

17. Minimize the following Boolean expression using K-map in (a) SOP form (b)POS form
    a. Y(A,B,C,D) = Σm (1,4,6,9,10,11,14,15) (7)
    b. Y(A,B,C,D) = ΠM (0,1,3,5,6,7,9,10,11,12,13,15) (8)

18. a. Design a BCD-Excess 3 code converter and implement it using logic gates. (8)
    b. Design a 2 bit magnitude comparator using logic gates. (7)

(OR)

19. Implement the following Boolean function using 8:1 MUX
    a. F(A,B,C,D)=A′BD′+ACD+ B′CD+A′C′D (8)
    b. F(A,B,C,D)= ∏M(0,3,5,8,9,10,12,14) (7)

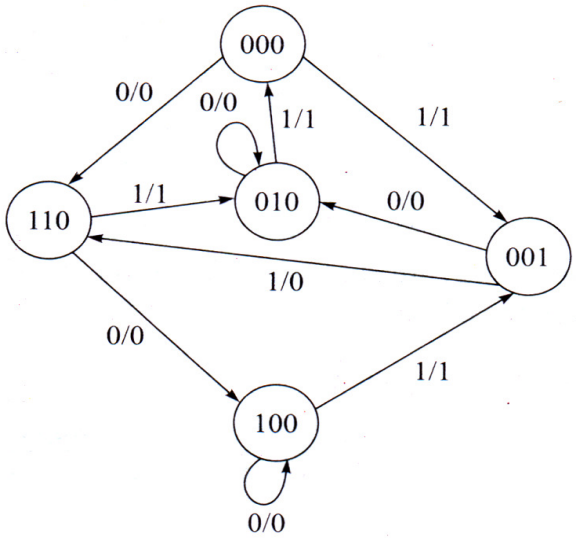
20. a. Explain the working of a master slave JK flip flop. (7)
    b. Draw a 4 bit Johnson counter using D flip flop and explain its operation. (8)

(OR)

21. Design a 3 bit (mod 8) synchronous UP-DOWN counter.
    When UP/DOWN=1→UP MODE
    UP/DOWN=0→DOWN MODE.

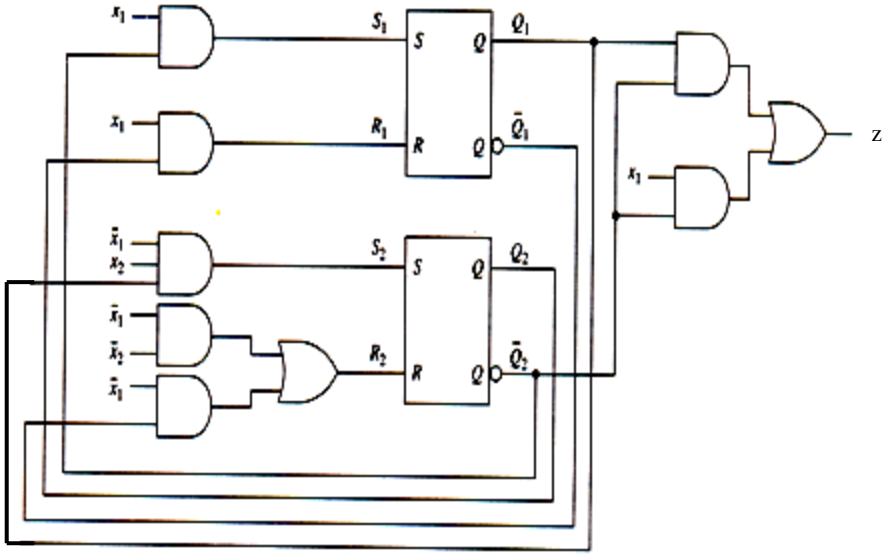
[P.T.O]

22. Design a sequential logic circuit using J-K flip-flops for the state diagram shown:



(OR)

23. Analyze the given Asynchronous sequential circuit and draw the flow diagram.



24. What are the types of PLDs? Explain with example.

(OR)

25. Explain TTL digital logic family in detail. How is it superior to RTL and DTL families? Draw the circuit of a TTL NAND gate and explain its operation.