Reg. No. _____

# Karunya University

**(Karunya Institute of Technology and Sciences)**

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

## End Semester Examination – April/May 2010

**Subject Title : DIGITAL ELECTRONICS** **Time : 3 hours**

**Subject Code: EC209** **Maximum Marks: 100**

---

## Answer ALL questions

## PART – A (10 x 1 = 10 MARKS)

1. Represent -9 with 8 bits in signed 1's complement representation.
2. State duality property of Boolean algebra.
3. Give the truth table of half subtractor.
4. What are universal gates?
5. Write the characteristic equation of JK flip flop.
6. What is a shift register?
7. How is T flip flop obtained from JK flip flop?
8. Define race condition.
9. State the difference between PLA and PAL.
10. Define fan out of any logic.

## PART – B (5 x 3 = 15 MARKS)

11. Express the Boolean function F=A+B'C in sum of minterms rotation.
12. Implement the following Boolean function using 4 to 1 Multiplexer.
    $F(A,B,C)= \sum(1,3,5,6)$
13. What is shift register? Draw the circuit of a serial input serial output shift register.
14. Compare Mealy and Moore models.
15. How write and read operations are performed in RAM?

## PART – C (5 x 15 = 75 MARKS)

16. a. Minimize the function
    $f(A,B,C,D)= \Pi M(0,1,2,3,4,7,8,11,12,14,15)$ (11)
    b. Convert: $(AA1)_{16}$ to decimal and octal numbers (4)

(OR)

17. a. Express f (A, B, C, D) =AB+A'BC+C'D as the SOP and the POS. (8)
    b. Prove the following Boolean identities
    i. A'O B= A⊕B b. A ⊕ B ⊕ A.B= A+B (7)

18. a. Implement a full adder adder with a decoder and two OR gates. (7)
    b. Design a 4 input priority encoder. (8)

(OR)

19. Write short notes on the following:
    a. 4 bit magnitude comparator. (10)
    b. Parity generation and checking. (5)

20. What is a Flip flop? Explain its types briefly.

(OR)

[P.T.O]

21. Give in detail about the following
    a. Timing signal generation in counters (7)
    b. Ring counter (8)

22. Design a synchronous Mod-5 counter using Master Slave JK flip flops to run through the states 010,011,100,101 and 110 only. Also realize the circuit using JK flip flop and basic gates.

(OR)

23. Obtain reduced flow table of a negative edge triggered T flip flop which has 2 inputs Toggle (T) and Clock (C) and one output Q. The output is complemented if T=1 and C changes from 1 to 0. Otherwise under any other input condition, the output Q remains unchanged.

24. Using PAL , Design a combinational circuit with Boolean functions

    $w(A,B,C,D) = \sum(2,12,13)$

    $x(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$

    $y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$

    $z(A,B,C,D) = \sum(1,2,8,12,13)$

(OR)

25. Discuss in detail about TTL gates.