Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – May / June 2009

Subject Title: DIGITAL ELECTRONICS **Time : 3 hours**
Subject Code: EC209 **Maximum Marks: 100**

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. Convert $(0.6875)_{10}$ to binary.
2. Name different types of codes.
3. Differentiate between an encoder and decoder.
4. What is the necessity for parity generation and checking?
5. Define excitation table.
6. Define shift register.
7. Give examples of two programmable logic devices.
8. Which are the two logic families no longer used in the design of digital systems?
9. What do a state table consists of?
10. Differentiate between synchronous and asynchronous sequential circuits.

PART – B (5 x 3 = 15 MARKS)

11. What is EBCDIC code and which code replace this type of code.
12. Draw the symbol, input & out put signal and truth table of 2-input AND gate.
13. Explain with logical diagram and functional table the SR latch with NOR gate.
14. What is state diagram? Explain with example.
15. What is ROM? Explain?

PART – C (5 x 15 = 75 MARKS)

16. Convert the following decimal numbers to their equivalent octal numbers.
    a. $(4429.635)_{10}$ b. $(791.125)_{10}$ c. $(11.9375)_{10}$ (5 +5+5)

(OR)

17. a. Find the canonical product of sum (POS) form and sum of product (POS) form of the function $F(A,B,C) = (\overline{A}).(B+\overline{C})$ (7+8)

    b. Minimize the Boolean function $F = \overline{ABC} + \overline{A}B\overline{C} + A\,\overline{BC} + AB\overline{C} = \sum(0,2,4,6)$ using k-map.

18. a. Design and explain the operation of a 4 bit binary adder? (7.5)
    b. Describe the working of a Binary to gray code converter. (7.5)

(OR)

19. a. Explain the full adder with block diagram and truth table. (5)
    b. Design an even parity generator and binary to seven segment display converter? (10)

20. a. Implement a RS flip flop using (i) NAND gate (ii) NOR gate and explain with truth table.(8)
    b. Explain a 4 bit ring counter using JK flip flop. (7)

(OR)

[P.T.O]

21. Write short notes on
    a. Up/Down Counter. (7)
    b. Shift registers using JK flip-flop. (8)

22. Design a sequential logic circuit that detects a pattern '01101' in a given input sequence bit streams.

(OR)

23. With the help of an example explain about.
    a. State reduction. (7.5)
    b. Asynchronous sequential logic. (7.5)

24. a. Draw a basic ECL circuit diagram and explain its working principle. (8)
    b. Draw a basic IIL circuit diagram and explain its working principle. (7)

(OR)

25. a. With the help of a suitable example explain how digital function are implemented using PAL22V10 device (8)
    b. Describe the operation of CMOS inverter (7)