Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)
(Anna University batch)

End Semester Examination – November / December 2008

Subject Title: DIGITAL ELECTRONICS **Time : 3 hours**
Subject Code: EC209 **Maximum Marks: 60**

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. Convert the binary number $(110100)_2$ into gray code.
2. Explain De-Morgan's theorem.
3. Perform half adder using 2x4 multiplexer.
4. _____ gate is used for half adder.
5. Name two asynchronous counters.
6. The number of flip-flops required for a Mod-16 ring counter are _____.
7. When the circuit is not controlled by the clock, the transition from one state to next occurs when ever there is a change in the input to the circuit at any time and hence this circuit is called as ___
8. _____ circuits are referred as finite state machine.
9. Fan-in of a logic gate is nothing but the _____
10. The fastest logic family is _____

PART – B (5 x 2 = 10 MARKS)

11. Convert $(274.2875)_{10}$ to binary.
12. Implement half adder using NAND gates only.
13. Differentiate combinational circuits and sequential circuits.
14. Define state change.
15. Define Propagation delay.

PART – C (5 x 8 = 40 MARKS)

16. Simplify the Boolean function f(A,B,C,D)= Σ(0,2,3,5,6,7,8,9) with 10,11,12,13,14,15 as don't cares

(OR)

17. Simplify and minimize the following four-variable switching function using Quine-McClusky tabulation method. f(A,B,C,D)= Σ(0,1,2,3,4,6,8,9,10,11)

18. Design a comparator, which compares the magnitude of two numbers X and Y, each consisting of two bits and giving three outputs F_1, F_2, F_3 such that
    F_1 = 1 if X>Y
    F_2 =1 if X=Y
    F_3=1 if X<Y

(OR)

19. Realize the function Σ(0,1,3,5,11,15) using multiplexer

20. Explain the working of master slave J-K flip-flop

(OR)

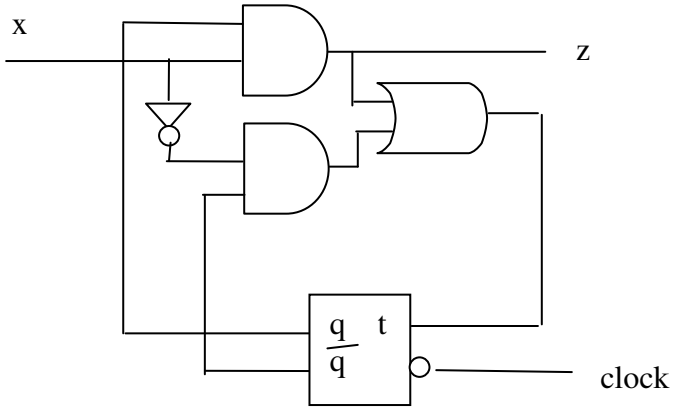
[P.T.O]

21. Design a synchronous Mod-5 counter using J-K flip-flop to run through the states 001,010,011,100 and 101 only.

22. Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected

(OR)

23. Analyse the synchronous sequential circuit shown in figure and draw the state diagram.



24. Implement the following Boolean expression using PLA

Y_1=ABC' +A'B

Y_2=A'B' +AC

(OR)

25. Explain the operation of TTL Nand gate.