Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November / December 2009

Subject Title: DIGITAL ELECTRONICS **Time : 3 hours**
Subject Code: EC209 **Maximum Marks: 100**

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. Convert the given Hexadecimal number $(B65F)_{16}$ into an equivalent decimal number.
2. Prove that x+1=1 using Boolean algebra postulates.
3. Implement NOT gate using NOR gate.
4. Draw the circuit of a half adder.
5. What is a flip-flop?
6. Mention the characteristic table of D flip-flop.
7. What is the use of state table?
8. Indicate the excitation table of T flip-flop.
9. The propagation delay of standard TTL is _____.
10. What is the main advantage of using Integrated Injection Logic (IIL)?

PART – B (5 x 3 = 15 MARKS)

11. Simplify the Boolean function F=x'yz + x'yz'+ xy'z'+ xy'z
12. Design a full adder circuit from its function table.
13. Draw the circuit of 4-bit ring counter and explain its operation.
14. What is the need for state reduction?
15. What are the various types of output configurations supported in TTL gates?

PART – C (5 x 15 = 75 MARKS)

16. Simplify the following Boolean functions using K-Map:
    a. $F(w,x,y,z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$
    b. $F(w,x,y,z) = \Sigma (1, 3, 7, 11, 15)$; $d(w,x,y,z) = \Sigma (0, 2, 5)$

(OR)

17. Simplify the following Boolean functions using Quine-McCluskey method.
    $F(w,x,y,z) = \Sigma (0, 1, 2, 8, 10, 11, 14, 15)$

18. Draw the combinational logic circuit of 4-bit magnitude comparator and explain its operation in detail.

(OR)

19. a. Design a 4 to 1 multiplexer circuit and explain its operation.
    b. Implement the given function using 4 x 1 multiplexer $F(A,B,C) = \Sigma (1, 3, 5, 6)$

20. With neat diagram, explain the operation of 4-bit binary ripple counter in detail.

(OR)

21. With neat diagram, explain the operation of synchronous BCD counter in detail.

22. Design a 3-bit synchronous counter with the proper excitation table using T flip-flop.

(OR)

23. Design a modulo-5 synchronous counter using J-K flip-flop.

24. A combinational circuit is defined by the functions: $F_1 (A, B, C) = \Sigma (3, 5, 6, 7)$
    $F_2 (A, B, C) = \Sigma (0, 2, 4, 7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs.

(OR)

25. With neat internal diagram, explain the operation of basic gate of Emitter Coupled Logic family.