Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November / December 2008

Subject Title: DIGITAL ELECTRONICS **Time : 3 hours**
Subject Code: EC209 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. The 2's complement representation of zero is ----------
2. Define : Minterm
3. The universal gates are ---------- and ----------
4. Define parity bit
5. Define sequential circuit
6. Name any two applications of shift registers
7. What is the difference between Moore and Mealy model of sequential circuit?
8. Define state reduction
9. What due you understand by PAL
10. Name any two logic families

PART – B (5 x 3 = 15 MARKS)

11. Find the complement of the given Boolean expression F1 = x(y' z' + yz)
    and F2 = x' y z' + x' y' z
12. Realize the basic gates using NAND gates
13. Define excitation table and draw the excitation table of T – flip - flop
14. Draw the state diagram and state table for a 2 bit binary counter
15. Define Fan - in, Noise immunity and Noise margin, Propagation delay

PART – C (5 x 15 = 75 MARKS)

16. Simplify the Boolean function by means of tabulation method
    $F(A,,B,C,D,E,F) = \sum (6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$

(OR)

17. Simplify the Boolean function F with the don't – care conditions d in (i) sum of products and (ii) product of sums
    $F (w,x,y,z) = \sum (0,1,2,3,7,8,10)$; $d(w,x,y,z) = \sum (5,6,11,15)$

18. Design a BCD to XS3 code converter using Decoder

(OR)

19. a. Implement the following function with a multiplexer (8)
    $F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$
    b. Design a 4 bit adder/subtractor (7)

20. With a neat schematic and timing diagram explain the operation of a 4 bit ripple counter

(OR)

21. Explain the operation of a 4 bit parallel in serial out shift register using JK FFs.
    The data input is 1011

[P.T.O]

22. A sequential circuit with two D flip – flops, A and B, two inputs, x and y and one output, z is specified by the following next-state and output equations:

$A(t+1) = x'y + xA$

$B(t+1) = x'B + xA$

$Z = B$

Draw the logic diagram of the circuit. Derive the state table and the state diagram

(OR)

23. Design a synchronous 3 - bit binary counter

24. a. Design a Full adder using PROM. (10)
    b. Explain the advantages of PLA. (5)

(OR)

25. a. Compare the performance of various logic families. (10)
    b. Explain the operation of MOS inverter with neat diagram. (5)