B.E (Etox) sem 7 (Rev.)
Elective-I - Microcomputer system Design. 28/12/07

Con/5654–07. (REVISED COURSE) CD–7107
(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data if **required**.
(4) Draw **neat diagrams** wherever **necessary**.

1.a) What is reflected wave switching? **04**
b) Explain instruction pairing rules for Pentium processor **04**
c) What is the difference between selection and reselection phases in SCSI? **04**
d) What are the functions of D1 stage of Pentium processor pipeline? **04**
e) Explain what is hidden bus arbitration in PCI bus. **04**

2.a) Draw state diagram of Pentium Bus cycles. Explain each state and its transition. **12**
b) What are special cycles in Pentium processor? **08**

3.a) Explain with a neat diagram data bus steering logic for 8 and 16 bit devices in Pentium processors **10**
b) Explain code cache organization of Pentium Processor and also explain what is split line access? **10**

4.a) Explain with the neat block diagram show the configuration of all components of PC and their respective connections. (CPU, PCI bus, Memory, Peripherals, ISA bus must be shown) **10**
b) Explain following PCI signals **10**
SDONE, SBO, STOP#, IDSEL#, DEVSEL#
(# : these signals are active low signals)

5.a) Explain following terms of USB bus **10**
- Host Controller and its functions
- Different types of data transfers

5.b) Explain how interrupts are routed in PCI bus? Explain with Suitable example. **10**

6.a) Explain Register model of IDE **06**
b) Explain following signals in SCSI **08**
ATN, MSG, BSY, SEL
c) Explain what is CHS addressing and LBA addressing in IDE. **06**

7. **Write Short notes on (Any Four)** **20**
1. System Management mode of Pentium Processor
2. Central resources for PCI based devices
3. Zone Bit Recording
4. Branch prediction Logic in Pentium
5. Interrupt acknowledge transaction in PCI