B.E. Sem 7 (Rev.) Microcomputer System Design. 29/12/08

Con. 5825-08. Extx.

(REVISED COURSE) **RC-7235**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **five** questions out of **remaining** questions.
(3) Illustrate **answers with sketches** wherever **required**.
(4) **Figures** to the **right** indicate **full** marks.
(5) Use **legible** handwriting. Use a **blue/black** ink pen to write answers. Use of **pencil** should be done only to draw **diagrams** and **graphs.**

1. (a) Explain what is Latency timer in PCI bus. **5**
   (b) Explain instruction pairing rules for Pentium Processor. **5**
   (c) Explain Bus Parking of PCI bus. **5**
   (d) Explain different USB transfer types. **5**

2. (a) Explain MESI model of Pentium data cache. **10**
   (b) Explain the function of following PCI signals :— **10**
   (i) IRDY# (iv) FRAME#
   (ii) IDSEL (v) LOCK#
   (iii) TRDY#
   (# : These signals are active low signals)

3. (a) Explain reflected wave switching and shared interrupts in PCI bus. **10**
   (b) Explain error-handling signals of Pentium Processor. **10**

4. (a) Explain SCSI bus phases with neat timing diagrams. **10**
   (b) Explain code cache organization of Pentium Processor and also explain what is split line access. **10**

5. (a) Explain register model of IDE, also explain what is CHS addressing and LBA addressing in IDE. **10**
   (b) Explain following terms of USB bus :— **10**
   (i) Host controller (iv) Transaction frame
   (ii) USB Hub (v) USB driver.
   (iii) NAK and ACK token

6. (a) Explain branch prediction logic in Pentium and D1 stage of Pentium processor pipeline. **10**
   (b) Explain bank conflict for simultaneous data access and clean line replacement in data cache of Pentium Processor. **10**

7. Write short notes on following :— **20**
   (a) System Management mode of Pentium
   (b) Zone Bit Recording
   (c) PCI hidden bus arbitration
   (d) Central Resources for PCI based devices.