

- N.B. :** (1) Question No. 1 is **compulsory**. Solve any **four** questions from remaining **six** questions.
 (2) Assume **suitable** data if **required**.
 (3) Draw **neat** diagrams wherever **necessary**.

- Q.1 a)** Explain why the code cache of Pentium processor is triple ported. 04
b) Explain methods of invalidating cache lines for Pentium processor. 04
c) What are the functions of D1 stage of Pentium processor pipeline? 04
d) What is the difference between selection and reselection phases in SCSI? 04
e) Explain what is Latency Timer in PCI bus. 04
- Q.2 a)** Draw Pentium Bus cycles for a burst cache line fill operation from external DRAM. Explain each signal and its significance. 12
b) What is system management mode in Pentium processor? 08
- Q.3 a)** Explain with a neat diagram data bus steering logic for 16 bit devices in Pentium processors and explain a 32-bit data read operation from the same device. 10
b) With respect to data cache of Pentium Processor explain following terms 10
- Clean line replacement
 - Bank conflict for simultaneous data access
- Q.4 a)** Explain with the neat block diagram show the configuration of all components of PC and their respective connections. (CPU, PCI bus, Memory, Peripherals, ISA bus must be shown) 10
b) Explain following PCI signals 10
IRDY#, TRDY#, FRAME#, PAR, DEVSEL#
 (# : these signals are active low signals)
- Q.5 a)** Explain following terms of USB bus 10
- Host Controller and its functions
 - NAK and ACK token
 - Transaction frame
- b)** Explain shared interrupts in PCI bus. Explain with Suitable example. 10
- Q.6 a)** Explain what is sector interleave and its use. 06
b) Explain following signals in SCSI 08
ATN, MSG, BSY, SEL
- c)** Explain protocol for data read / write commands in IDE. 06
- Q.7 Write Short notes on (Any Three) 20**
1. Hidden Bus arbitration in PCI bus
 2. Zone Bit Recording
 3. Branch prediction Logic in Pentium
 4. Bus parking in PCI
 5. Reflected wave switching