Library) B.E. (Etrx) Sem-VIII (Rev. 5/6/07.

Elective II: VLSI Design.

P4/RT-Ex-07-21

Con. 2931-07. **[REVISED COURSE]** **ND–1801**

(3 Hours) **[Total Marks : 100**

N.B: 1) Question **No.1** is **compulsory**
2) Attempt any **four** out of remaining six questions
3) Assume suitable data wherever **necessary**

1.(a) Explain the switching characteristics of CMOS gate. Suggest the methods to improve the switching performance. [10]

(b) Design one bit full adder using AND, OR, EXOR gates. Write the verilog description of the circuit. Write the stimulus for the full adder [10]

2.(a) Discuss in detail 4 x 4 array multiplier. Can this be used as a building block to create an 8 x 8 multiplier ? If so detail the problems and modifications that need to be made. [10]

(b) Explain EEPROM using floating gate NMOSFETS. [10]

3.(a) Construct a circuit diagram for a CMOS logic gate that implements the AOI function F = A [B + C (D+E)] Design the W/L ratio for the transistors [10]

(b) Design CMOS implementation of JK flip flop .Explain what are the limitations of your design. [10]

4.(a) Summarize the approach you would take to reduce the power dissipation of a CMOS chip that is designed for palm top computer. [10]

(b) What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100pF of on-chip load to satisfy the metal migration consideration (J_{AL} = 0.5 mA/μ)? What is the ground bounce with the chosen Conductor size. The module is 500μm from both the power and the ground Pads and the supply voltage is 5 volts. The rise/fall time of the clock is 1 nsec.(Assume R_s = .05Ω/sq) [10]

5.(a) Discuss floor planning and routing in VLSI. [10]

(b) What is cross talk in integrated circuits? Discuss various methods to reduce it. [10]

6.(a) Explain three main approaches to Design for Testability in detail [10]

(b) Explain in detail Pipelined system design [10]

7 Write short notes on any three :- [20]

a. Behavioral and RTL modeling
b. Resistance and Capacitance Estimation
c. Clock generation and Distribution
d. Carry Look ahead adders