B.E. sem 8 (Rev.) Etrx Elective II – VLSI Design 05/6/

Con. 3452-08. CO-4099

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary**.

1. (a) Give the various scan based technique and explain how serial scan testing is implemented for testing the chip. **10**
   (b) Discuss in detail 4 × 4 array multiplier. **10**

2. (a) State various important parameters affecting the switching performance of CMOS circuit. Suggst the methods to improve the switching performance. **10**
   (b) Design CMOS implementation of JK Flip-Flop. Explain what are the limitations of your design. **10**

3. (a) Give the various sources of power dissipation in digital CMOS circuits and explain the methods to reduce power dissipation. **10**
   (b) Explain the following as applied to verilog HDL. **10**
      (i) RTL and Behavioural modeling.
      (ii) Gate level modeling.

4. (a) Write the verilog code for 4 Bit Counter and 4 Bit Full adder with carry look ahead. **10**
   (b) Discuss the three main approaches to Design for testability. **10**

5. (a) What is cross talk in integrated circuits ? Explain various methods to reduce it. **10**
   (b) Discuss floor planning and routing in chip design in detail. **10**

6. (a) Discuss the fault models in CMOS and explain stuck at one (S_{a_1}), stuck at zero (S_{a_0}) faults with respect to 2 input CMOS NAND gate. **10**
   (b) Explain the system level test techniques in detail. **10**

7. Write short notes on any **three** :— **20**
   (a) Low power design issues
   (b) Clock generation and distribution
   (c) Resistance and capacitance estimation
   (d) Layout design for improved testability.