(Library). Sem-VIII [Rev] ETRX.
Elective II : VLSI Design.

25/5/09.

Con. 3006-09.   **VR-4179**

(REVISED COURSE)

(3 Hours)   [Total Marks : 100

N.B : (1) Question No.1 is **Compulsory**.
    (2) Attempt any **four** out of remaining **six** questions.
    (3) Assume **suitable data** wherever **necessary**.

1. (a) Explain various sources of power dissipation in digital CMOS circuits and explain **10** the methods to reduce power dissipation.

  (b) Discuss in detail 4 x 4 array multiplier. Can this be used as a building block to create **10** an 8 x 8 multiplier ? If so detail the problems and modifications that need to be made.

2. (a) Explain the different types of physical fault that can occur in a CMOS chip and **10** relate them to a typical circuit failure.

  (b) Explain EEPROM using floating gate NMOSFETS.   **10**

3. (a) Summarize the approach you would take to reduce the power dissipation of a CMOS **10** chip that is designed for palm top computer.

  (b) What would be the conductor width of power and ground wires to a 50 MHz clock **10** buffer that drives 100pF of on-chip load to satisfy the metal migration consideration $(J_{AL} = 0.5$ mA/μ)? What is the ground bounce with the chosen Conductor size. The module is 500 μm from both the power and the ground Pads and the supply voltage is 5 volts. The rise/fall time of the clock is 1 nsec.(Assume $R_s = .05$ Ω/sq).

4. (a) Construct a circuit diagram for a CMOS logic gate that implements the AOI function **10** F = A [B + C (D + E)] Design the W/L ratio for the transistors.

  (b) Design CMOS implementation of JK flip flop. Explain what are the limitations **10** of your design.

5. (a) Discuss floor planning and routing in VLSI.   **10**
  (b) Explain in detail Pipelined system design.   **10**

6. (a) Explain three main approaches to Design for Testability in detail.   **10**
  (b) What is cross talk in integrated circuits ? Discuss various methods to reduce it.   **10**

7. Write short notes on any **three** :—   **20**
    (a) Behavioral and RTL modeling
    (b) Low power design considerations
    (c) Clock generation and Distribution
    (d) Carry Look ahead adders.

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