

Con. 6144-11.

(REVISED COURSE) Advance VLSI Design MP-5170

(3 Hours)

[Total Marks : 100

- N. B. :** (1) Question No. 1 is **compulsory**.
 (2) Answer any **four** out of remaining **six** questions.
 (3) Assume any **suitable** data wherever required and justify the **same**.
1. A. An nFET with $L=0.5\mu\text{m}$ is built in a process where $K_n'=100\mu\text{A/V}^2$ and $V_{tn}=0.7\text{V}$. The gate to source voltage is set to a value of $V_{GSn}=V_{DD}=3.3\text{V}$. Calculate the required channel width to obtain a resistance of $R_n=950\Omega$ (use value of $\eta=1$). 5
 - B. Draw analog design octagon and explain its significance. 5
 - C. Explain pipelined design concept. 5
 - D. Explain low power design considerations. 5
 2. A. What is the cell ratio and pull up ratio of 6T SRAM cell. How does these affect the read/write operation. 10
 - B. Explain cross coupled differential sense amplifier with circuit diagram which is used in SRAM cell. State the advantages over other differential sense amplifiers. 10
 3. A. What are the parasitic elements of interconnect wire and how it affects electrical behavior of the circuit. 10
 - B. Explain modeling of RC delay of interconnect wire using distributed RC model. How this delay can be reduced? 10
 4. A. What are the requirements of a clock signal and list the points to be considered in clock distribution. 10
 - B. What are the different clocking strategies employed in VLSI systems. Discuss 'H tree' clock distribution in high density CMOS circuits. 10
 5. A. Implement 4 bit adder using Carry Look Ahead (CLA) principle. 10
 - B. Stat the need of input and output circuit. Explain with neat diagram the schematic and design considerations for the same. 10
 6. A. Explain EEPROM using floating gate NMOSFET 10
 - B. What is cross talk in integrated circuits? Explain various methods to reduce it. 10
 7. A. Implement the following function using NOR-NOR implementation for a PLA
 i) $Y1 = ab + a'c$
 ii) $Y2 = a'bc + abc$
 iii) $Y3 = a'b + ac$ 10
 - B. Explain the need of frequency compensation in operational amplifiers. 10