Karunya University
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)
(Anna University batch)

End Semester Examination – November / December 2008

Subject Title: DIGITAL INTEGRATED CIRCUITS   Time : 3 hours
Subject Code: IT212   Maximum Marks: 60

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. _____ is the Maximum external noise voltage added to an input signal that does not cause an unreliable change in circuit design.
2. Adding inverters to all inputs & outputs of an AND gate produces the_____ logic Junction.
3. In digital logic circuit, the total propagation time is equal to the _____ of typical gate times, the number of _____ in the circuit.
4. _____ is the logic circuit that produces a coded output corresponding to the highest valued input.
5. The two types of shift register counters are _____.
6. An unwanted voltage or current spike of short duration is known as _____ .
7. ECL is used for _____ applications because its speed is superior.
8. The T TL gates in all the available series are in three types of output configuration that are

   _____, _____, _____
9. The time required to complete a write operation is called as _____.
10. Refreshing circuitry is required for _____ RAM.

PART – B (5 x 2 = 10 MARKS)

11. State demorgan's laws
12. How can a decoder be converted into demultiplexer .
13. What are the applications of Shift register?
14. Define Fan in & Fan out
15. What is meant by combinational PLD?

PART – C (5 x 8 = 40 MARKS)

16. Simplify by using karnaugh map
    F= $\sum_M$ (0,1,4,5,6,11,14,15,16,17,20,22,30,32,33,36,37,48,49,52,53,59,63)
                              (OR)
17. Draw a NAND logic diagram that implement the complements of the following function

    (a) F(A,B,C,D) = $\sum$(0,1,2,3,4,8,9,12)   (b) A$\overline{B}$ +ABD+AB$\overline{D}$ + $\overline{A}\overline{C}\overline{D}$ + $\overline{A}\overline{B}\overline{C}$

18. Design a Combinational circuit generate the 9's Complement of a BCD digit.
                              (OR)
19. Construct a 16 X 1 mux with two 8 X 1 and one 2 X 1 Multiplexers. [Use block diagrams]

20. Explain in detail about TTL logic circuits operation and its three variable O/P configurations.
                              (OR)
21. Draw & Explain in detail about CMOS Transmission Gate circuits and its characteristics.

22. Explain EPROM and PLA in detail.
                              (OR)
23. Draw a RAM Cell & explain its working .write short notes on ROM.

24. Define flip flops & Explain the types of flip-flops.
                              (OR)
25. Design a counter with the following repeated binary sequence 0,1,2,3,4,5,6. Use J;K flip-flops.