Reg. No. _____

Karunya University

End Semester Examination – November/December 2010

Subject Title: **DIGITAL INTEGRATED CIRCUITS** **Time: 3 hours**
Subject Code: **IT212** **Maximum Marks: 100**

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. Convert $(26)_8$ into $(?)_2$.
2. What is the expansion of EBCDIC and ASCII?
3. What are universal gates? Why are they called so?
4. Draw a half subtractor circuit.
5. How many flipflops are required to construct decade counter?
6. Write the truthtable of D-flipflop.
7. Which is the fastest of all logic families?
8. Which type of TTL gate can drive CMOS gates?
9. How is erasing operation performed in the EPROM?
10. Are PLAs and FPLAs volatile or nonvolatile?

PART – B (5 x 3 = 15 MARKS)

11. Perform the subtraction using 2's complement method.
    a. 01000 – 01001   b. 01100 – 00011
12. $F = ABC + B\overline{C}D + \overline{A}BC$. Realize using logic gates.
13. What is meant by race around condition in flipflops.
14. Define the terms fan-out and fan-in.
15. What is the basic memory cell used in static RAMs. Does it require refreshing?

PART – C (5 x 15 = 75 MARKS)

16. a. Perform the following
        i) 375 = ( )$_8$ = ( )$_2$ ii) 2's Complement of 01100100
        iii) Represent + 25 in 1's complement (6)
    b. Minimize f(A,B,C,D) = Σm (1,3,5,8,9,11,15) + d(2,13) using k-map. (9)
                             (OR)
17. a. Convert
        i) $Y = (A + B)(A + C)(B + \overline{C})$ into standard POS form using Boolean algebra.
        ii) $Y = AB + A\overline{C} + BC$ into standard SOP using Boolean algebra. (6)
    b. A staircase light is controlled by two switches, one at the top of the stairs and another at
        the bottom of the stairs. (i) Make truth table for this system (ii) Write the logic equation
        in SOP form. (iii) Realize the circuit using AND-OR gate. (9)

18. a. Explain the working of 4 bit binary adder/subtractor circuit. (9)
    b. Draw a magnitude comparator circuit and explain it. (6)
                             (OR)
19. a. Implement a logic function f (A, B, C, D) = Σ(1, 2, 6, 13, 15) using multiplexer. (9)
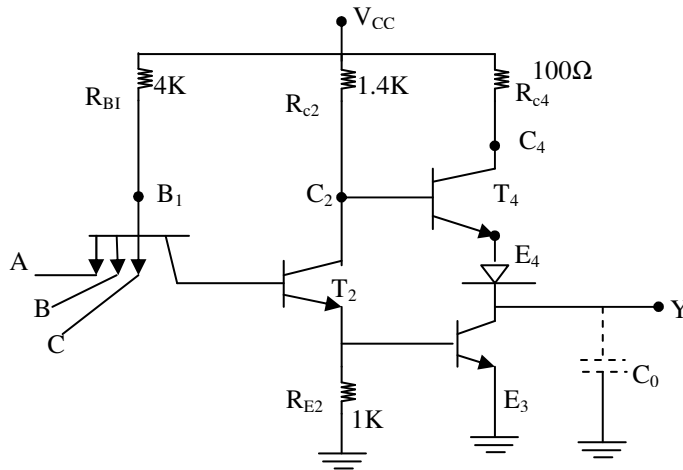   b. Describe 3 to 8 line decoder circuit. (6)

[P.T.O]

20. Explain the working of clocked RS and clocked D flip-flop.

(OR)

21. Design a counter to count the following sequence (7,4,8,3,9,2,10,1,11,0,7…..) using JK flip-flops.

22. a. Explain the operation of TTL gate with active pull-up shown in figure.   (9)

   b. Is it possible to drive CMOS gates with TTL gates? If no, suggest a suitable method to achieve this.   (6)

(OR)

23. Explain the working of emitter coupled logic.

24. A combinational circuit is defined by the function
    $F_1(A,B,C) = \Sigma(3,5,6,7)$ $F_2(A,B,C) = \Sigma(0,2,4,7)$. Implement the circuit with a PLA having three inputs, 4 product terms and two outputs.

(OR)

25. a. Explain the concept of memory decoding.   (9)
    b. Write short notes on types of memories.   (6)