Reg. No. _____

Karunya University

(Karunya Institute of Technology and Sciences)

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – April/May 2010

Subject Title: DIGITAL INTEGRATED CIRCUITS **Time: 3 hours**

Subject Code: IT212 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. Represent the number 98.72 in power of 10.
2. Give the expression for Distributive law.
3. Define combinational logic circuit.
4. What is the use of magnitude comparator?
5. State the main difference between lathes and flip flops.
6. How many flip flops are required to build a binary counter that counts from 0 to 1023?
7. What is the other name of speed-power product?
8. Draw the circuit of CMOS inverter.
9. What are the two parameters that are used in digital systems?
10. What is FPGA?

PART – B (5 x 3 = 15 MARKS)

11. Convert 5A9.B4H to binary.
12. Draw the general structure of decoder.
13. What are the three parameters to be considered in designing digital systems with flip flops?
14. Mention the logic levels of TTL, ECL, and CMOS families.
15. List the features of EPROM.

PART – C (5 x 15 = 75 MARKS)

16. Simplify the following three variable expressions using Boolean algebra. $Y=\Pi M (3, 5, 7)$.

(OR)

17. Reduce the following function using Karnaugh map technique and implement using basic gates.
$f(A,B,C,D=\overline{A}\,\overline{B}D+AB\overline{C}\,\overline{D}+\overline{A}BD+ABC\overline{D})$

18. Explain the principle and operation of 1:4 demutiplexer with its truth table and logic diagram.

(OR)

19. Design and explain the operation of binary to gray code converter with its K-map and logic diagram.

20. Draw the basic block diagram of two bit synchronous binary counter and discuss the timing diagram. Also discuss about state sequence of 3 bit synchronous binary counter.

(OR)

21. Describe the operation of S-R latch and D-latch with the aid of its truth table and diagrams.

22. Mention the features of Emitter Coupled Logic. Explain the operation of two input ECL gate with necessary diagrams.

(OR)

23. What is meant by wire- AND connection in Resistor- Transistor logic gate? Draw the circuit diagram of RTL and explain the operation.

24. Implement the following Boolean function using ROM.
$F1(A1,A0)=\Sigma m(1,2)$ $F2(A1,A0)=\Sigma m(0,1,3)$. Also explain the operation of ROM.

(OR)

25. Draw the block diagram of sequential programmable logic device and explain its operation in detail.