Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – May / June 2009

Subject Title: DIGITAL INTEGRATED CIRCUITS **Time : 3 hours**
Subject Code: IT212 **Maximum Marks: 100**

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. The binary number 110010111 has an ---------- parity.
2. $(532.78)_{10} = (?)_8$
3. What are logic gates? Name the three basic logic gates.
4. A data selection is also called a ----------
5. Why a JK flip flop is called a Universal Flip-flop?
6. A 4-bit UP/DOWN binary ripple counter is initially reset to 0000. The UP/DOWN mode select terminal designated as $\overline{U}$/D on the pin connection diagram of the IC is tied to HIGH input. What will be the counter output status after the first clock pulse?
7. Define Fan-out.
8. State the logic levels of ECL.
9. The process of storing new information into memory is referred to as a memory ---------- operation.
10. How many 32K X 8 RAM chips are needed to provide a memory capacity of 256K bytes?

PART – B (5 x 3 = 15 MARKS)

11. Simplify the following expression: Y= (A+B) (A'+C) (B'+C')
12. Briefly describe the functional principle of ROM.
13. Classify shift registers.
14. Draw the CMOS inverter diagram.
15. Design a 32 X 8 ROM with its internal logic diagram.

PART – C (5 x 15 = 75 MARKS)

16. Reduce the following function using K- map technique. f (A,B,C,D) = ∑m(0,1,4,8,9,10)

(OR)

17. Write a short notes on i) BCD ii) ASCII iii) EBCDIC

18. Describe the principle and operation of 1:4 demultiplexer with the use of function table.

(OR)

19. Design a BCD to Excess 3 code converter with the help of Karnaugh map reduction technique.

20. Illustrate the working of clocked JK Flip-flop by using input and output waveforms.

(OR)

21. Discuss the operation of 3-bit synchronous binary counter. Draw the timing diagram with state sequence.

22. What is TTL logic? Explain the working of two input TTL NAND gate with circuit diagram. State the standard TTL characteristics.

(OR)

23. Draw and explain the operation of RTL and DTL circuits with its gate specifications.

24. Implement the following two Boolean function with a PLA:
    X= AB'+AC+A'BC'
    Y= (AC+BC)'

(OR)

25. Explain the sequential programmable devices in detail with its block diagram.