Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November / December 2008

Subject Title: DIGITAL INTEGRATED CIRCUITS **Time : 3 hours**
Subject Code: IT212 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. Convert $(FACE)_{16}$ into Binary.
2. Prove that A+AB=A.
3. Draw the logic symbol of XNOR gate.
4. A decoder with enable input can function as a _____
5. Flip Flops operate with signal levels are referred as _____
6. Write the characteristic equation of JK FF
7. Construct an IC diode from Transistor
8. _____ is a nonsaturated digital logic family.
9. Memory unit stores binary information in groups of bits called _____
10. PAL has _____ AND array and _____ OR array.

PART – B (5 x 3 = 15 MARKS)

11. Explain Duality principle with an example
12. Give the truth table of Priority Encoder
13. Obtain T-flipflop from (i) JK flipflop and (ii) D flipflop
14. Give the basic circuit of NMOS NOR gate.
15. Draw the logic diagram of Memory cell

PART – C (5 x 15 = 75 MARKS)

16. a. Perform X - Y and Y - X using 10's complement (5)
    X=72532
    Y=3250
    b. Add 732 and 398 using BCD (4)
    c. Minimize the given expression using K-Map (6)
    F = A'B'C' + B'CD' + A'BCD' + AB'C'

(OR)

17. a. Find the complements of the functions F_1 and F_2 (4)
    F_1=x'yz'+x'y'z
    F_2=x (y'z'+yz)
    b. Define and prove Consensus Theorems. (6)
    c. Express the Boolean Function F= xy + x'z in product of maxterm form. (3)
    d. Write the operator precedence for evaluating Boolean expression. (2)

18. a. With a neat block diagram, explain the operation of 4 bit Binary Adder- Subtractor (6)
    b. Implement a Full Adder with decoder circuit. (4)
    c. Explain a 3 bit even parity generator. (5)

(OR)

[P.T.O]

19. a. With Truth table and Circuit diagram explain the operation of Octal to Binary encoder. (9)
    b. Implement the given combinational function using MUX of your choice
    Y=AB+A'CD+B'CD' (6)

20. a. With a neat circuit, analyse the operation of D-type positive edge triggered Flipflop. (8)
    b. Explain the operation of Serial adder using D FF. (7)

(OR)

21. a. Design synchronous BCD counter with T FFs. (10)
    b. Give any two ways to achieve BCD counter using Counter with parallel load. (5)

22. a. Define Noise Margin. (3)
    b. Explain the operation of basic RTL NOR gate. (5)
    c. How will you construct Exclusive-OR gate with CMOS transmission gate. (7)

(OR)

23. a. Explain CMOS as Inverter, NOR and NAND. (12)
    b. Write the applications of open collector TTL gate. (3)

24. a. Explain Memory decoding in detail. (12)
    b. Give the steps for WRITE operation in random access memory (3)

(OR)

25. a. Define Combinational PLD. (2)
    b. Give the basic configurations of three combinational PLDs (6)
    c. Design a combinational circuit using ROM, the circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. (7)