Reg. No. _____

Karunya University

(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November / December 2009

Subject Title: DIGITAL INTEGRATED CIRCUITS **Time : 3 hours**
Subject Code: IT212 **Maximum Marks: 100**

Answer ALL questions

PART – A (10 x 1 = 10 MARKS)

1. Write the expansion for ASCII.
2. What are canonical forms?
3. What are universal gates?
4. Data selector is also called_____.
5. Basic building block of the sequential logic circuit is _____.
6. Write any 2 uses of counters.
7. High speed digital logic family is _____.
8. Define fan out.
9. Power consumption is high in SRAM (true or false)
10. What is PAL?

PART – B (5 x 3 = 15 MARKS)

11. State De Morgans theorem.
12. Design a half adder circuit.
13. Write the characteristics table of D-flip flop.
14. Mention the special characteristics of digital logic families.
15. Draw the configuration of PROM.

PART – C (5 x 15 = 75 MARKS)

16. a. $(110101.1110)_2 = (\ \ )_8$ (2)
    b. $(650)_{10} = (\ \ )_{16}$ (2)
    c. $(0.011)_2 = (\ \ )_{10}$ (2)
    d. Represent +6132.789 in floating point (2)
    e. Write short notes on error detecting codes. (7)

(OR)

17. a. Simplify $F(w,x,y,z)= \sum(0,1,4,5,8,9)$ using karnaugh map. (8)
    b. Simplify the expression AB+A(B+C)+B(B+C) using Boolean algebra techniques. (7)

18. Design a 3 to 8 line decoder.

(OR)

19. a. Draw the block diagram of two bit magnitude comparator and design the same. (10)
    b. Design a 2 bit odd parity generator. (5)

20. a. Draw a clocked JK flip flop using AND and NOR gates (5)
    b. Explain the operation of serial in-parallel out shift register using D flip flop with necessary diagram (10)

(OR)

21. a. Design a 4 bit binary ripple counter using 'T' flip flop (10)
    b. Draw the Logic diagram of a ring counter (5)

22. Explain the operation of three state TTL gate with necessary diagram

(OR)

23. Discuss the operation of
    a. CMOS NAND gate (7½)
    b. CMOS NOR gate (7½)

24. Implement the following two Boolean functions with a PLA
    F1= AB′ +AC+A′ B C′
    F2= AC+BC

(OR)

25. Draw the general structure of 4 inputs, 4 AND arrays and 4 outputs PAL.