

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code: IT-801A

ADVANCED COMPUTER ARCHITECTURE

Time Allotted: 3 Hours

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Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A (Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:

 $10 \times 1 = 10$

What will be the speed up for a 4 segment linear
pipeline when the number of instruction $n = 64$?

a) 4.5

b) 3.82

c) 8-16

d) 2.95.

ii) Virtual address can be divided into some fixed size fields of

a) segments

b) blocks

c) pages

d) tags.

ii) Which is not the property of a memory module?

a) Inclusion

b) Capability

c) Locality

d) Consistency.

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iv)	iv) In absence of TLB, to access a physic						memo	ry
	loca	tion in	a page-	memo	ry sys	stem ho	w mai	ny
	men	nory acce	sses are	require	ed?			
	a)	1		b)	2			
	c)	3		d)	4.			
v)	A pi	peline sta	ige					
	a)	is seque	itial circi	uit				
	b)	is combin	national	circuit				
	c)	both (a)	and (b)					
	d)	none of t	hese.					
vi)	Which of the following is not the possible cause of							
	data	hazard ?)	•				
	a)	RAW		b)	RAR	7		
	c)	WAW		d)	WAR.			
vii)		time to					same	in
		ch of			ng s	hared	memo	ry
		tiprocesso	or models		7			
	a)	UMA		b)	COM			
	c)	SIMD		d)	NUM.			
viii)	viii) Utilization pattern of successive stages							а
	synchronous pipeline can be specified by							
	a)	Reservat		,		table		
	•	Excitatio)	•				_
ix)		ay proces	ssing is	possi	ble in	ı which	type	OI
		cessor?		1	3.713.77	_		
	1.40	SIMB		b)	MIMI			
	c)	MISD	:	•	SISD		c	
X)		flict miss	is occur	rea in	. wnici	n type o	memo	гу
7	_	oping?	ai a tima	ы	Dimoo			
	•	Set association		•	Direc	these.		
	CJ	Associati	.ve	aj	All OI	uicse.		
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GROUP – B (Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

- 2. Compare, Superscalar, Superpipeline and superscalar superpipelined processor.
- 3. Explain Flynn's classification of computers with suitable diagrams.
- 4. Explain the main factors influencing the performance of interconnection networks.
- 5. Assume a main memory of size 32K × 12, Cache memory of size 512 × 12 and block size of 1 word. For direct mapping what would be the size of the tag and index fields? Explain Data Hazard with example. 3 + 2
- 6. Explain S access and C access memory organization.

GROUP – C (Long Answer Type Questions)

Answer any three of the following. $3 \times 15 = 45$

7. Consider the following reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the Pipeline. Find out the simple and greedy cycle and MAL. If the pipeline clock rate is 25 MHz then what is the throughput of the pipeline? What are the bonds on MAL? 3+3+3+3+3

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- 8. a) Differentiate between multiprocessors and multicomputers based on their resource sharing, structure and processor communication.
 - b) Explain 10 subsystems in lightly coupled multiprocessor system with neat sketch. $7\frac{1}{2} + 7\frac{1}{2}$
- 9. a) How does cache memory effect the throughput of a computer system?
 - b) Distinguish between Write back and Write through cache.
 - c) What is the effect of memory bandwidth over effective memory access time?
 - d) What is cache coherence? How can we overcome this problem? 3+5+4+3
- 10. a) Compare the advantages and disadvantages of Direct mapping and Associative mapping.
 - b) A system with four way set associative cache has 128 blocks in the cache memory, each block contains 16 words (8 bit words) and the main memory has 16384 words. How many blocks are there in the main memory and what is the size of tag field?
 - c) Explain locality of reference.

5 + 5 + 5

11. Write short notes on any three of the following:

 $3 \times 5 = 15$

- a) Omega Network
- b) Array processor
- c) Reservation table
- d) Multiport network
- e) Power PC.

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