# ELECTRONIC DEVICES - I

1. Energy Bands in Solids
2. Energy Band Diagram
3. Metals, Semiconductors and Insulators
4. Intrinsic Semiconductor
5. Electrons and Holes
6. Doping of a Semiconductor
7. Extrinsic Semiconductor
8. N-type and P-type Semiconductor
9. Carrier Concentration in Semiconductors
10. Distinction between Intrinsic and Extrinsic Semiconductors
11. Distinction between Semiconductor and Metal
12. Conductivity of a Semiconductor

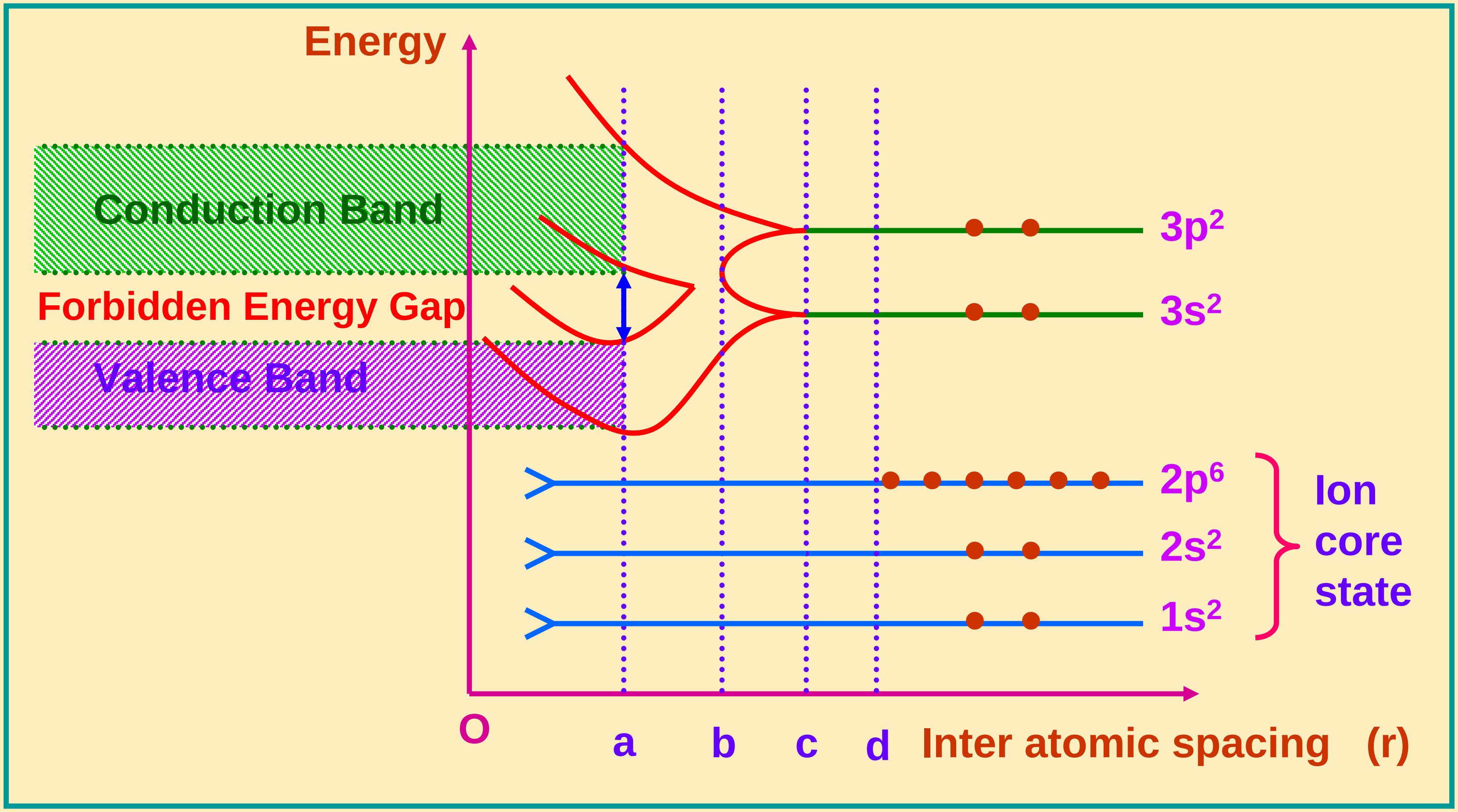
# Energy Bands in Solids:

- **According to Quantum Mechanical Laws, the energies of electrons in a free atom can not have arbitrary values but only some definite (quantized) values.**
- **However, if an atom belongs to a crystal, then the energy levels are modified.**
- **This modification is not appreciable in the case of energy levels of electrons in the inner shells (completely filled).**
- **But in the outermost shells, modification is appreciable because the electrons are shared by many neighbouring atoms.**
- **Due to influence of high electric field between the core of the atoms and the shared electrons, energy levels are split-up or spread out forming energy bands.**

**Consider a single crystal of silicon having N atoms. Each atom can be associated with a lattice site.**

**Electronic configuration of Si is $1s^2$, $2s^2$, $2p^6$,$3s^2$, $3p^2$. (Atomic No. is 14)**

## Formation of Energy Bands in Solids:



**(i) r = Od (>> Oa):**

Each of N atoms has its own energy levels. The energy levels are identical, sharp, discrete and distinct.

The outer two sub-shells (3s and 3p of M shell or n = 3 shell) of silicon atom contain two s electrons and two p electrons. So, there are 2N electrons completely filling 2N possible s levels, all of which are at the same energy.

Of the 6N possible p levels, only 2N are filled and all the filled p levels have the same energy.

**(ii) Oc < r < Od:**

There is no visible splitting of energy levels but there develops a tendency for the splitting of energy levels.

**(iii) r = Oc:**

The interaction between the outermost shell electrons of neighbouring silicon atoms becomes appreciable and the splitting of the energy levels commences.

**(iv) Ob < r < Oc:**

The energy corresponding to the s and p levels of each atom gets slightly changed. Corresponding to a single s level of an isolated atom, we get 2N levels. Similarly, there are 6N levels for a single p level of an isolated atom.

Since N is a very large number (≈ $10^{29}$ atoms / $m^3$) and the energy of each level is of a few eV, therefore, the levels due to the spreading are very closely spaced. The spacing is ≈ $10^{-23}$ eV for a 1 $cm^3$ crystal.

The collection of very closely spaced energy levels is called an **energy band**.

**(v) r = Ob:**

The energy gap disappears completely. 8N levels are distributed continuously. We can only say that 4N levels are filled and 4N levels are empty.

**(v) r = Oa:**

The band of 4N filled energy levels is separated from the band of 4N unfilled energy levels by an energy gap called **forbidden gap** or **energy gap** or **band gap**.

The lower completely filled band (with valence electrons) is called the **valence band** and the upper unfilled band is called the **conduction band**.

**Note:**

1. The exact energy band picture depends on the relative orientation of atoms in a crystal.
2. If the bands in a solid are completely filled, the electrons are not permitted to move about, because there are no vacant energy levels available.

# Metals:

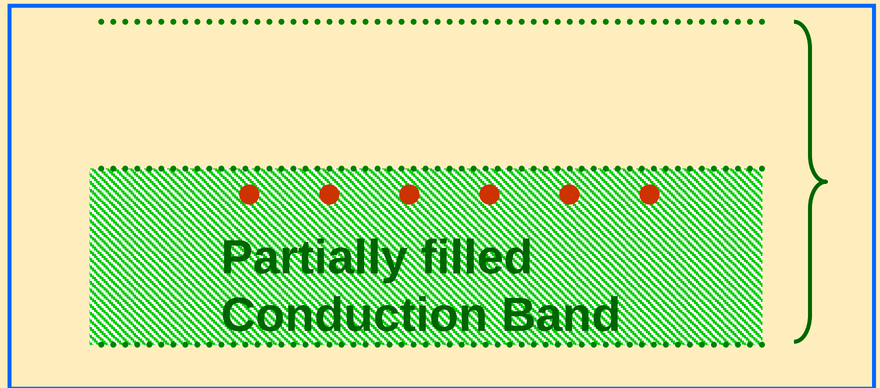
The first possible energy band diagram shows that the conduction band is only partially filled with electrons.

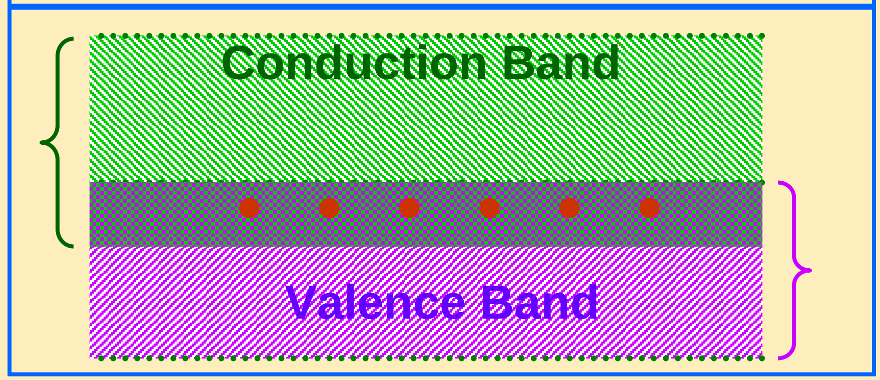
With a little extra energy the electrons can easily reach the empty energy levels above the filled ones and the conduction is possible.

The second possible energy band diagram shows that the conduction band is overlapping with the valence band.

This is because the lowest levels in the conduction band needs less energy than the highest levels in the valence band.

The electrons in valence band overflow into conduction band and are free to move about in the crystal for conduction.



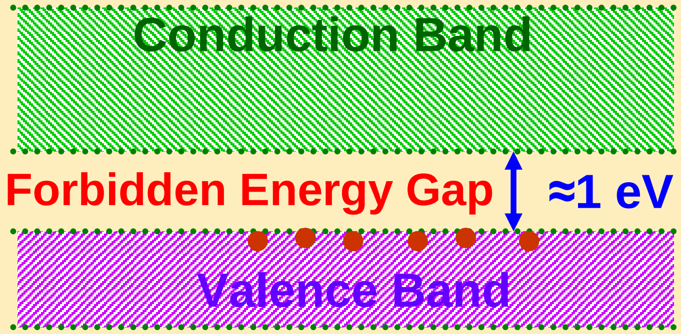

The highest energy level in the conduction band occupied by electrons in a crystal, at absolute 0 temperature, is called Fermi Level.

The energy corresponding to this energy level is called Fermi energy.

If the electrons get enough energy to go beyond this level, then conduction takes place.

# Semiconductors:

At absolute zero temperature, no electron has energy to jump from valence band to conduction band and hence the crystal is an insulator.




At room temperature, some valence electrons gain energy more than the energy gap and move to conduction band to conduct even under the influence of a weak electric field.

$E_{g\text{-}Si} = 1.1$ eV    $Eg_{Ge} = 0.74$ eV

The fraction is $p \propto e^{-\frac{E_g}{k_B T}}$

Since $E_g$ is small, therefore, the fraction is sizeable for semiconductors.

As an electron leaves the valence band, it leaves some energy level in band as unfilled.

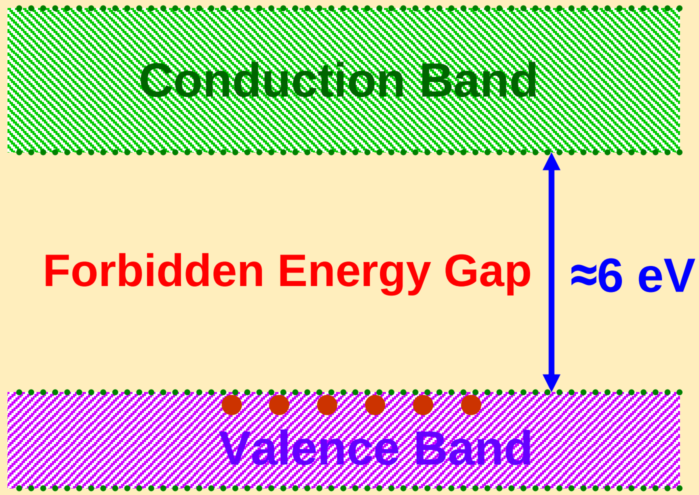
Such unfilled regions are termed as 'holes' in the valence band. They are mathematically taken as positive charge carriers.

Any movement of this region is referred to a positive hole moving from one position to another.

## Insulators:

Electrons, however heated, can not practically jump to conduction band from valence band due to a **large energy gap**. Therefore, conduction is not possible in insulators.

$E_{g\text{-}Diamond} = 7\ eV$




## Electrons and Holes:

On receiving an additional energy, one of the electrons from a covalent band breaks and is free to move in the crystal lattice.

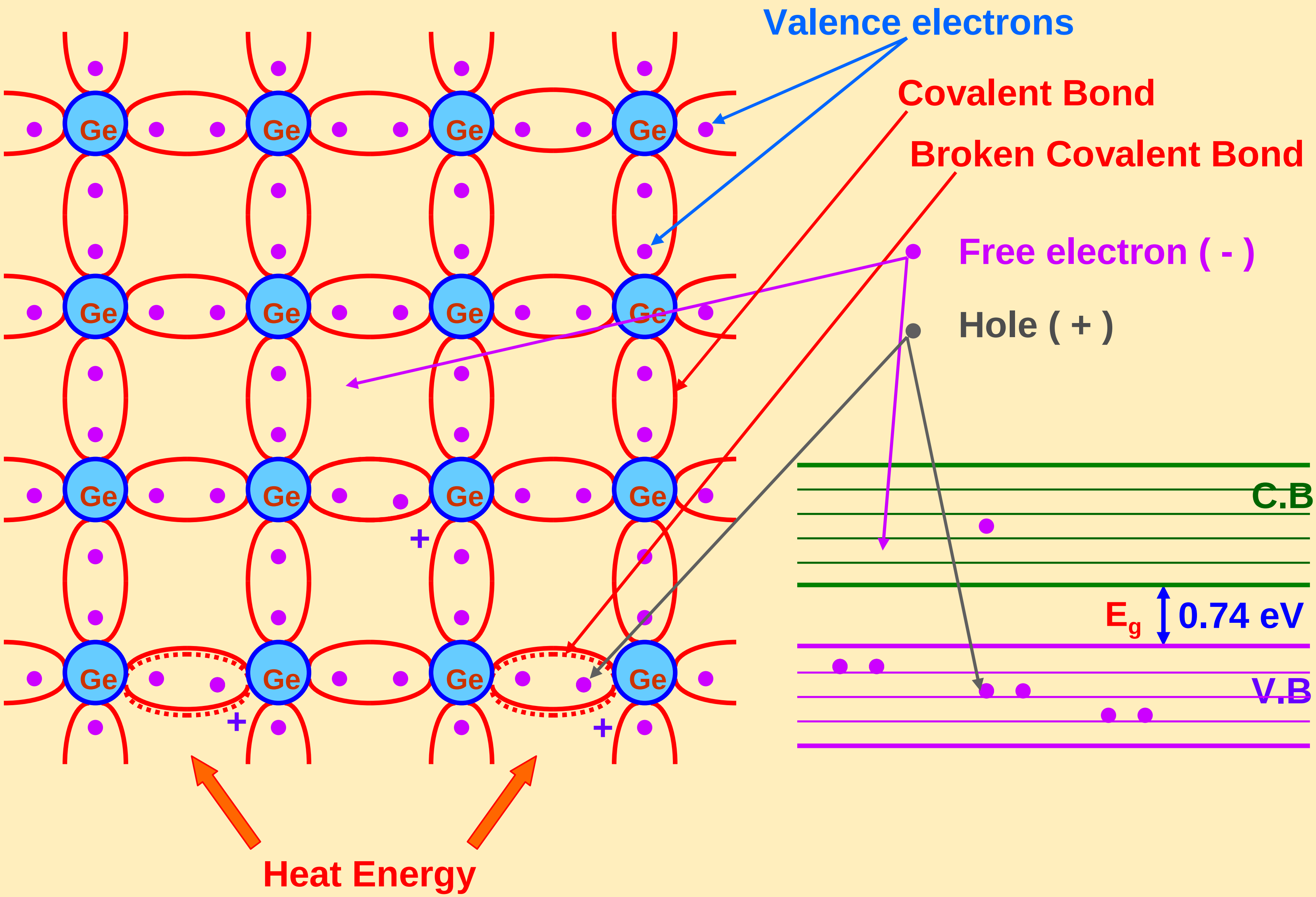
While coming out of the covalent bond, it leaves behind a vacancy named 'hole'.

An electron from the neighbouring atom can break away and can come to the place of the missing electron (or hole) completing the covalent bond and creating a hole at another place.

The holes move randomly in a crystal lattice.

The completion of a bond may not be necessarily due to an electron from a bond of a neighbouring atom. The bond may be completed by a conduction band electron. i.e., free electron and this is referred to as 'electron – hole recombination'.

# Intrinsic or Pure Semiconductor:



**Intrinsic Semiconductor is a pure semiconductor.**

**The energy gap in Si is 1.1 eV and in Ge is 0.74 eV.**

**Si: $1s^2, 2s^2, 2p^6, 3s^2, 3p^2$. (Atomic No. is 14)**

**Ge: $1s^2, 2s^2, 2p^6, 3s^2, 3p^6, 3d^{10}, 4s^2, 4p^2$. (Atomic No. is 32)**

**In intrinsic semiconductor, the number of thermally generated electrons always equals the number of holes.**

**So, if $n_i$ and $p_i$ are the concentration of electrons and holes respectively, then $n_i = p_i$.**

**The quantity $n_i$ or $p_i$ is referred to as the 'intrinsic carrier concentration'.**

# Doping a Semiconductor:

**Doping is the process of deliberate addition of a very small amount of impurity into an intrinsic semiconductor.**

**The impurity atoms are called 'dopants'.**

**The semiconductor containing impurity is known as 'impure or extrinsic semiconductor'.**

## Methods of doping:

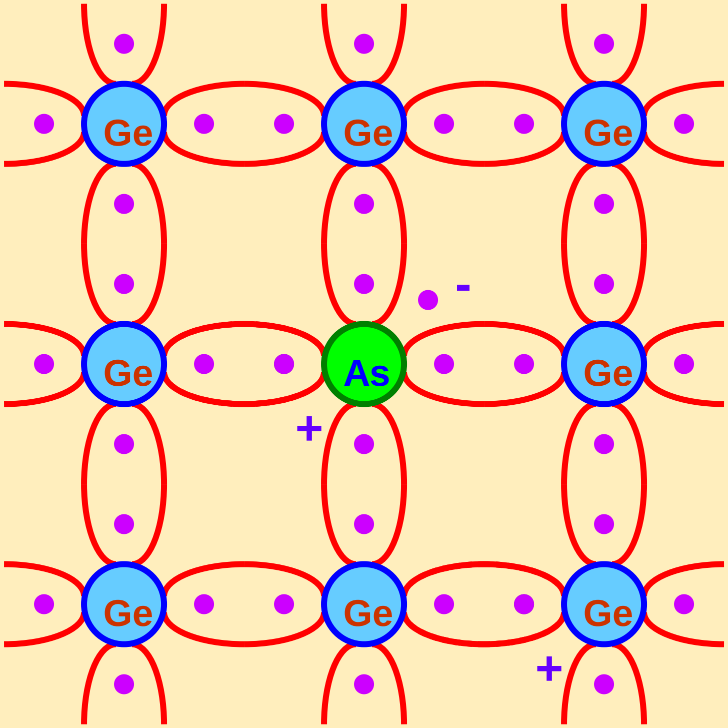
i) **Heating the crystal in the presence of dopant atoms.**

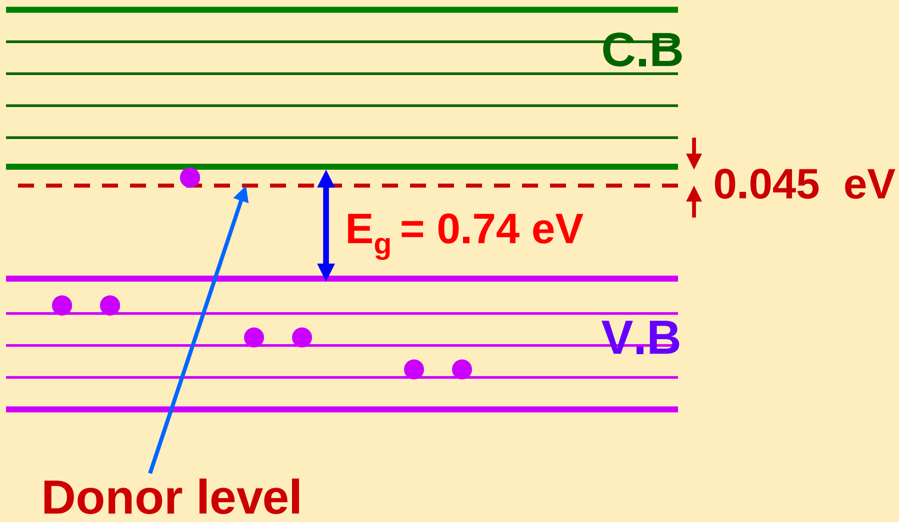
ii) **Adding impurity atoms in the molten state of semiconductor.**

iii) **Bombarding semiconductor by ions of impurity atoms.**

## Extrinsic or Impure Semiconductor:

### N - Type Semiconductors:




When a semiconductor of Group IV (tetra valent) such as Si or Ge is doped with a penta valent impurity (Group V elements such as P, As or Sb), N – type semiconductor is formed.

When germanium (Ge) is doped with arsenic (As), the four valence electrons of As form covalent bonds with four Ge atoms and the fifth electron of As atom is loosely bound.

**The energy required to detach the fifth loosely bound electron is only of the order of 0.045 eV for germanium.**

**A small amount of energy provided due to thermal agitation is sufficient to detach this electron and it is ready to conduct current.**

**The force of attraction between this mobile electron and the positively charged (+ 5) impurity ion is weakened by the dielectric constant of the medium.**

**So, such electrons from impurity atoms will have energies slightly less than the energies of the electrons in the conduction band.**

**Therefore, the energy state corresponding to the fifth electron is in the forbidden gap and slightly below the lower level of the conduction band.**

**This energy level is called 'donor level'.**

**The impurity atom is called 'donor'.**

**N – type semiconductor is called 'donor – type semiconductor'.**

## Carrier Concentration in N - Type Semiconductors:

**When intrinsic semiconductor is doped with donor impurities, not only does the number of electrons increase, but also the number of holes decreases below that which would be available in the intrinsic semiconductor.**

**The number of holes decreases because the larger number of electrons present causes the rate of recombination of electrons with holes to increase.**

**Consequently, in an N-type semiconductor, free electrons are the majority charge carriers and holes are the minority charge carriers.**

**If n and p represent the electron and hole concentrations respectively in N-type semiconductor, then**

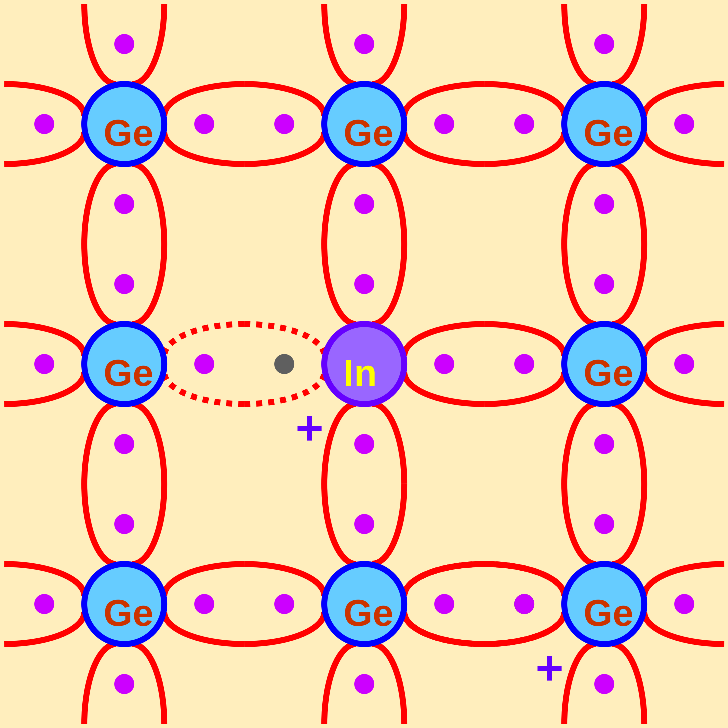
$$\boxed{n\,p = n_i\,p_i = n_i^2}$$

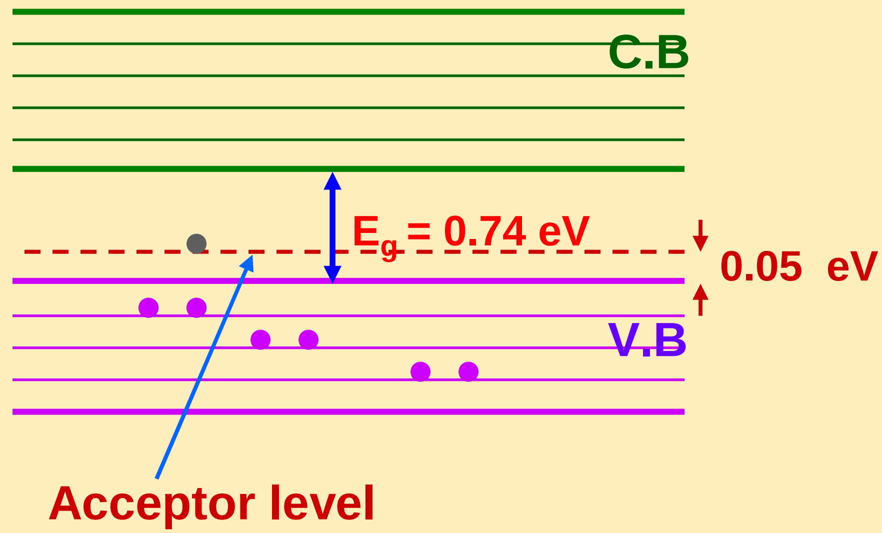
**where $n_i$ and $p_i$ are the intrinsic carrier concentrations.**

**The rate of recombination of electrons and holes is proportional to n and p. Or, the rate of recombination is proportional to the product np. Since the rate of recombination is fixed at a given temperature, therefore, the product np must be a constant.**

**When the concentration of electrons is increased above the intrinsic value by the addition of donor impurities, the concentration of holes falls below its intrinsic value, making the product np a constant, equal to $n_i^2$.**

# P - Type Semiconductors:




When a semiconductor of Group IV (tetra valent) such as Si or Ge is doped with a tri valent impurity (Group III elements such as In, B or Ga), P – type semiconductor is formed.

When germanium (Ge) is doped with indium (In), the three valence electrons of In form three covalent bonds with three Ge atoms. The vacancy that exists with the fourth covalent bond with fourth Ge atom constitutes a hole.

The hole which is deliberately created may be filled with an electron from neighbouring atom, creating a hole in that position from where the electron jumped.

Therefore, the tri valent impurity atom is called 'acceptor'.

Since the hole is associated with a positive charge moving from one position to another, therefore, this type of semiconductor is called
P – type semiconductor.

The acceptor impurity produces an energy level just above the valence band.

This energy level is called 'acceptor level'.

The energy difference between the acceptor energy level and the top of the valence band is much smaller than the band gap.

Electrons from the valence band can, therefore, easily move into the acceptor level by being thermally agitated.

P – type semiconductor is called 'acceptor – type semiconductor'.

In a P – type semiconductor, holes are the majority charge carriers and the electrons are the minority charge carriers.

It can be shown that, $\boxed{n\,p = n_i\,p_i = n_i^2}$

## Distinction between Intrinsic and Extrinsic Semiconductor:

| S. No. | Intrinsic SC | Extrinsic SC |
|---|---|---|
| 1 | Pure Group IV elements. | Group III or Group V elements are introduced in Group IV elements. |
| 2 | Conductivity is only slight. | Conductivity is greatly increased. |
| 3 | Conductivity increases with rise in temperature. | Conductivity depends on the amount of impurity added. |
| 4 | The number of holes is always equal to the number of free electrons. | In N-type, the no. of electrons is greater than that of the holes and in P-type, the no. holes is greater than that of the electrons. |

# Distinction between Semiconductor and Metal:

| S. No. | Semiconductor | Metal |
|---|---|---|
| 1 | Semiconductor behaves like an insulator at 0 K. Its conductivity increases with rise in temperature. | Conductivity decreases with rise in temperature. |
| 2 | Conductivity increases with rise in potential difference applied. | Conductivity is an intrinsic property of a metal and is independent of applied potential difference. |
| 3 | Does not obey Ohm's law or only partially obeys. | Obeys Ohm's law. |
| 4 | Doping the semiconductors with impurities vastly increases the conductivity. | Making alloy with another metal decreases the conductivity. |

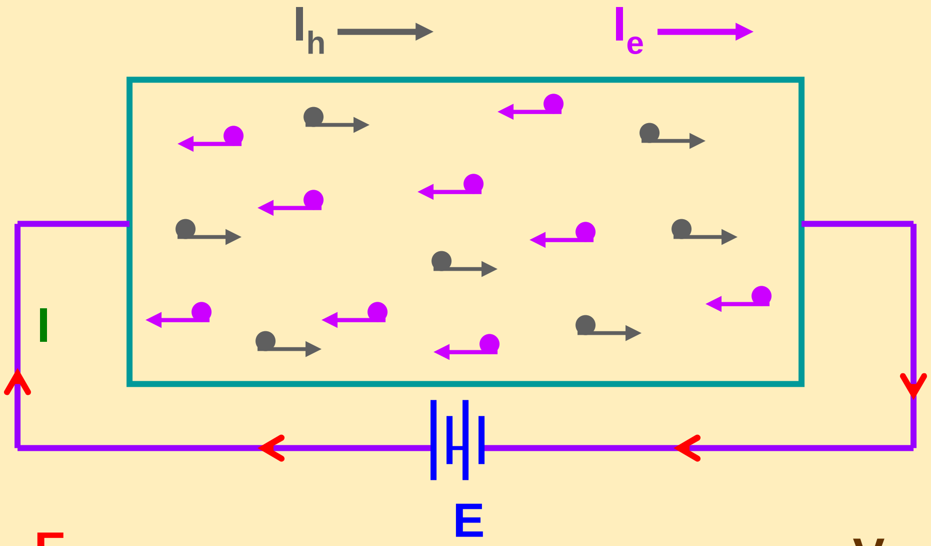
# Electrical Conductivity of Semiconductors:

$I = I_e + I_h$

$I_e = n_e e A v_e$ $\qquad$ $I_h = n_h e A v_h$

So, $I = n_e e A v_e + n_h e A v_h$

If the applied electric field is small, then semiconductor obeys Ohm's law.




$$\therefore \frac{V}{R} = n_e e A v_e + n_h e A v_h$$

$$= eA(n_e v_e + n_h v_h)$$

Or $$\frac{V A}{\rho l} = eA(n_e v_e + n_h v_h)$$

since $R = \dfrac{\rho l}{A}$

$$\frac{E}{\rho} = e(n_e v_e + n_h v_h)$$ since $E = \dfrac{V}{l}$

Mobility ($\mu$) is defined as the drift velocity per unit electric field.

$$\therefore \frac{1}{\rho} = e(n_e \mu_e + n_h \mu_h)$$

Or $$\boxed{\sigma = e(n_e \mu_e + n_h \mu_h)}$$

Note:

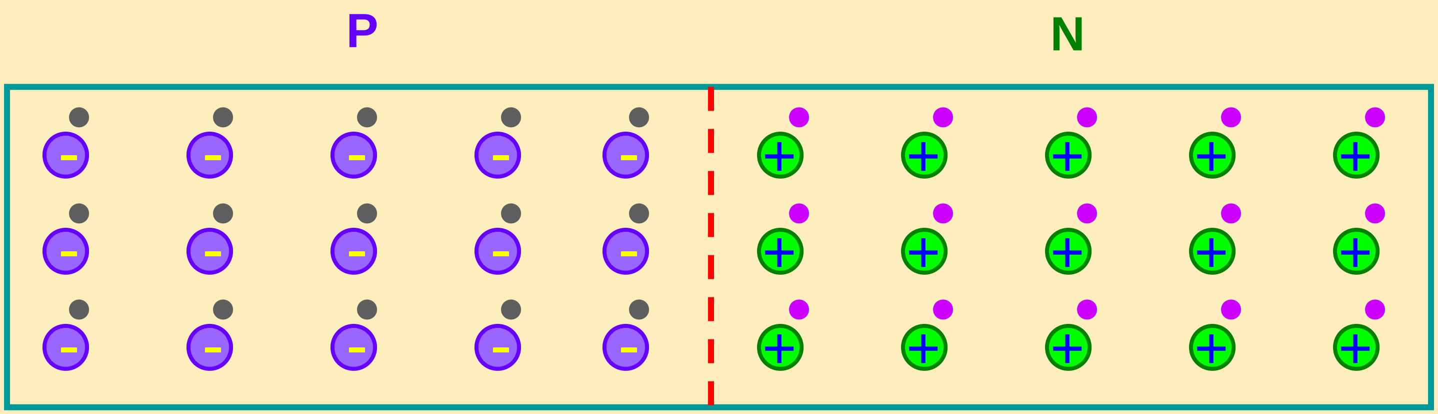
1. The electron mobility is higher than the hole mobility.
2. The resistivity / conductivity depends not only on the electron and hole densities but also on their mobilities.
3. The mobility depends relatively weakly on temperature.

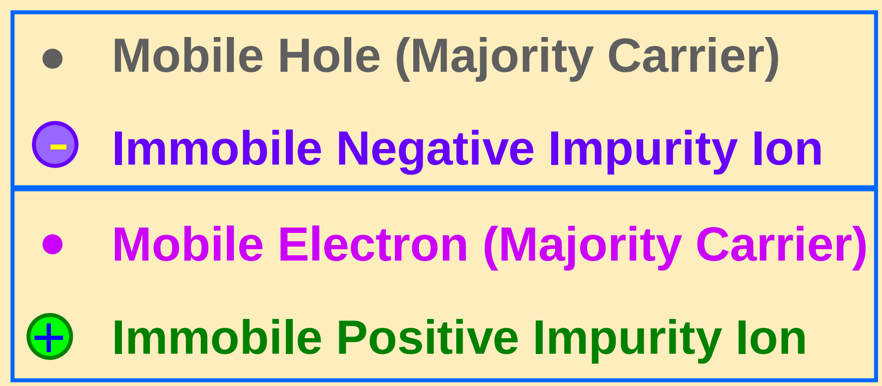
# ELECTRONIC DEVICES - II

1. PN Junction Diode
2. Forward Bias of Junction Diode
3. Reverse Bias of Junction Diode
4. Diode Characteristics
5. Static and Dynamic Resistance of a Diode
6. Diode as a Half Wave Rectifier
7. Diode as a Full Wave Rectifier

## PN Junction Diode:

When a P-type semiconductor is joined to a N-type semiconductor such that the crystal structure remains continuous at the boundary, the resulting arrangement is called a PN junction diode or a semiconductor diode or a crystal diode.



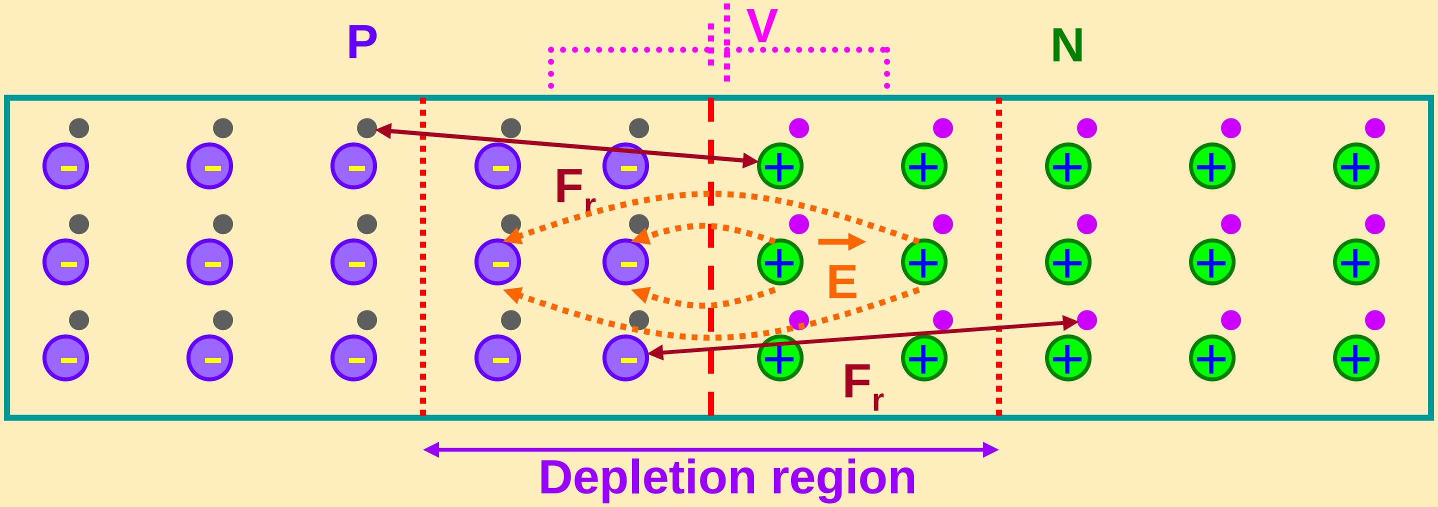

When a PN junction is formed, the P region has mobile holes (+) and immobile negatively charged ions.

N region has mobile electrons (-) and immobile positively charged ions.

The whole arrangement is electrically neutral.

For simplicity, the minority charge carriers are not shown in the figure.

# PN Junction Diode immediately after it is formed :




After the PN junction diode is formed –

i) Holes from P region diffuse into N region due to difference in concentration.

ii) Free electrons from N region diffuse into P region due to the same reason.

iii) Holes and free electrons combine near the junction.

iv) Each recombination eliminates an electron and a hole.

v) The uncompensated negative immobile ions in the P region do not allow any more free electrons to diffuse from N region.

vi) The uncompensated positive immobile ions in the N region do not allow any more holes to diffuse from P region.

vii) The positive donor ions in the N region and the negative acceptor ions in the P region are left uncompensated.

viii) The region containing the uncompensated acceptor and donor ions is called 'depletion region' because this region is devoid of mobile charges.

Since the region is having only immobile charges, therefore, this region is also called 'space charge region'.

ix) The N region is having higher potential than P region.

x) So, an electric field is set up as shown in the figure.

xi) The difference in potential between P and N regions across the junction makes it difficult for the holes and electrons to move across the junction. This acts as a barrier and hence called 'potential barrier' or 'height of the barrier'.

xii) The physical distance between one side and the other side of the barrier is called 'width of the barrier'.

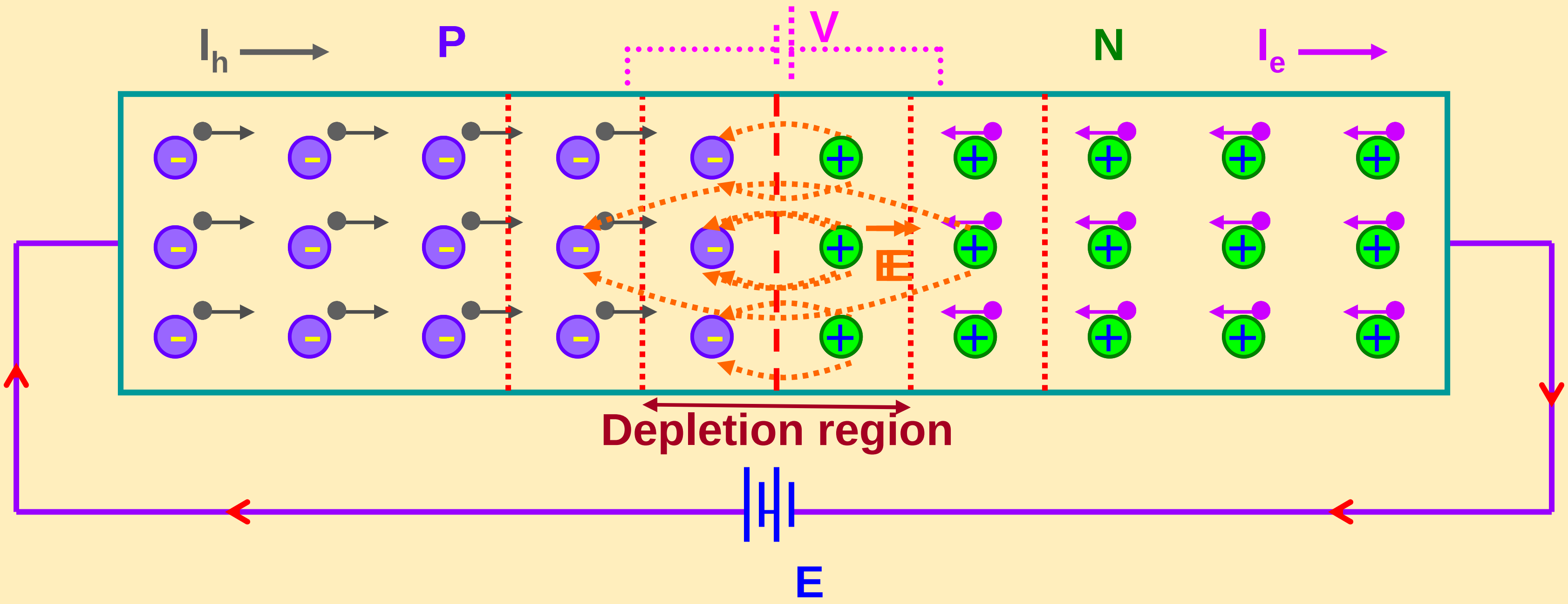
xiii) Potential barrier for Si is nearly 0.7 V and for Ge is 0.3 V.

xiv) The potential barrier opposes the motion of the majority carriers.

xv) However, a few majority carriers with high kinetic energy manage to overcome the barrier and cross the junction.

xvi) Potential barrier helps the movement of minority carriers.

# Forward Bias:




When the positive terminal of the battery is connected to P-region and negative terminal is connected to N-region, then the PN junction diode is said to be forward-biased.

i) Holes in P-region are repelled by +ve terminal of the battery and the free electrons are repelled by –ve terminal of the battery.

ii) So, some holes and free electrons enter into the depletion region.

iii) The potential barrier and the width of the depletion region decrease.

iv) Therefore, a large number of majority carriers diffuse across the junction.

v) Hole current and electronic current are in the same direction and add up.

v) Once they cross the junction, the holes in N-region and the electrons in P-region become minority carriers of charge and constitute minority current.

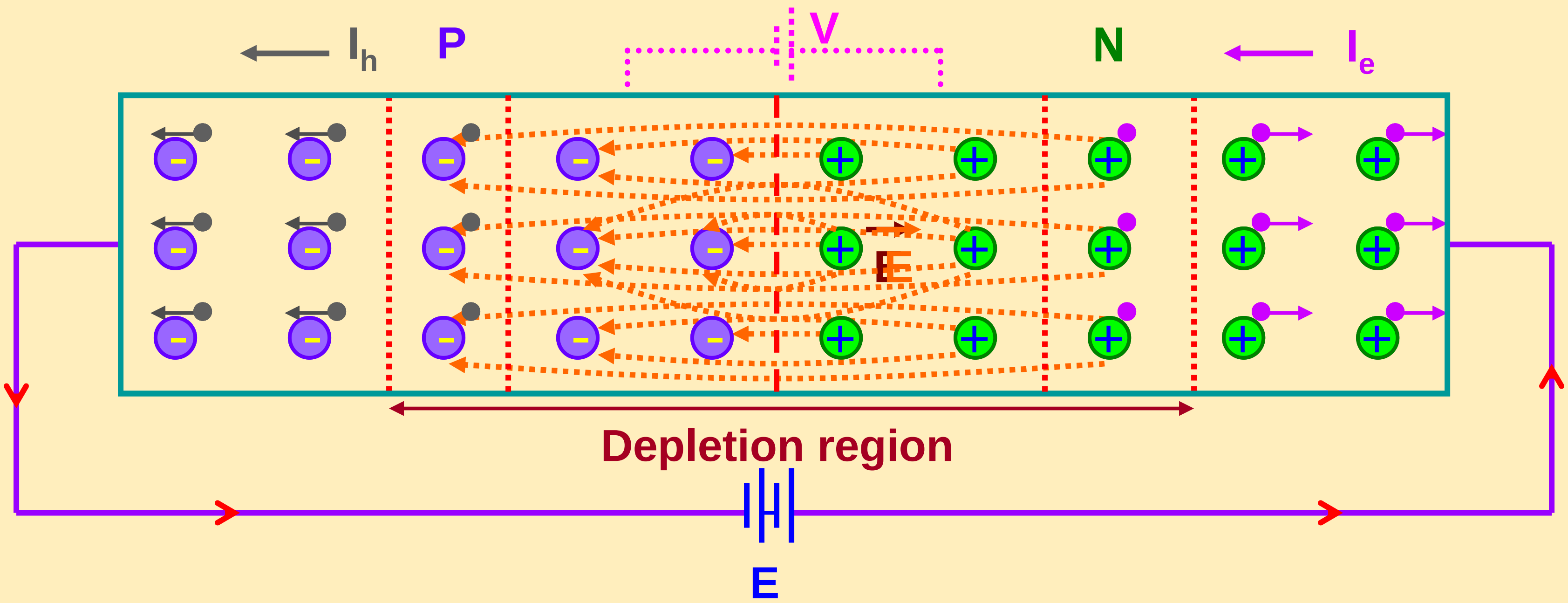
vi) For each electron – hole recombination, an electron from the negative terminal of the battery enters the N-region and then drifts towards the junction.

In the P-region, near the positive terminal of the battery, an electron breaks covalent bond in the crystal and thus a hole is created. The hole drifts towards the junction and the electron enters the positive terminal of the battery.

vii) Thus, the current in the external circuit is due to movement of electrons, current in P-region is due to movement of holes and current in N-region is due to movement of electrons.

viii) If the applied is increased, the potential barrier further decreases. As a result, a large number of majority carriers diffuse through the junction and a larger current flows.

# Reverse Bias:




When the negative terminal of the battery is connected to P-region and positive terminal is connected to N-region, then the PN junction diode is said to be reverse-biased.

i) Holes in P-region are attracted by -ve terminal of the battery and the free electrons are attracted by +ve terminal of the battery.

ii) Thus, the majority carriers are pulled away from the junction.

iii) The potential barrier and the width of the depletion region increase.

iv) Therefore, it becomes more difficult for majority carriers diffuse across the junction.

v) But the potential barrier helps the movement of the minority carriers. As soon as the minority carriers are generated, they are swept away by the potential barrier.

vi) At a given temperature, the rate of generation of minority carriers is constant.

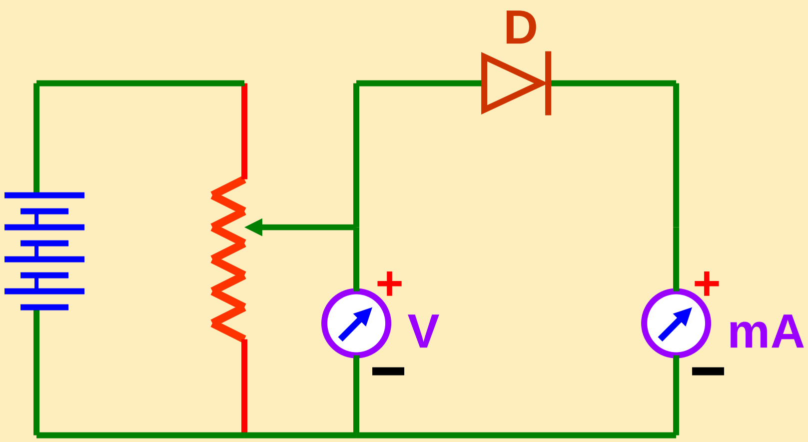
vii) So, the resulting current is constant irrespective of the applied voltage. For this reason, this current is called 'reverse saturation current'.

viii) Since the number of minority carriers is small, therefore, this current is small and is in the order of $10^{-9}$ A in silicon diode and $10^{-6}$ A in germanium diode.

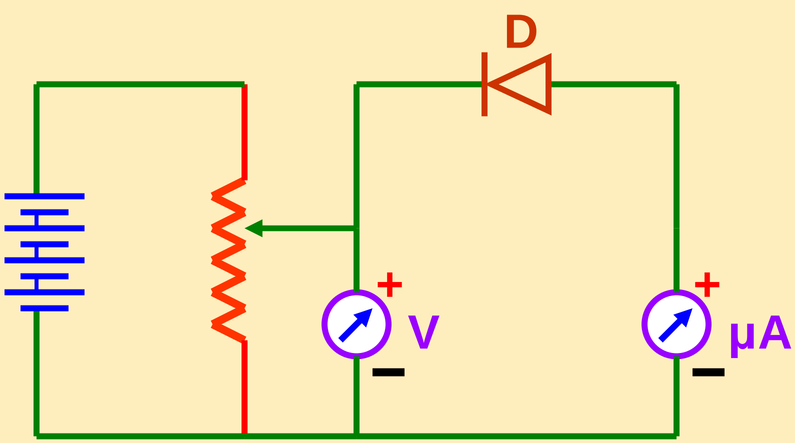
ix) The reverse – biased PN junction diode has an effective capacitance called 'transition or depletion capacitance'. P and N regions act as the plates of the capacitor and the depletion region acts as a dielectric medium.

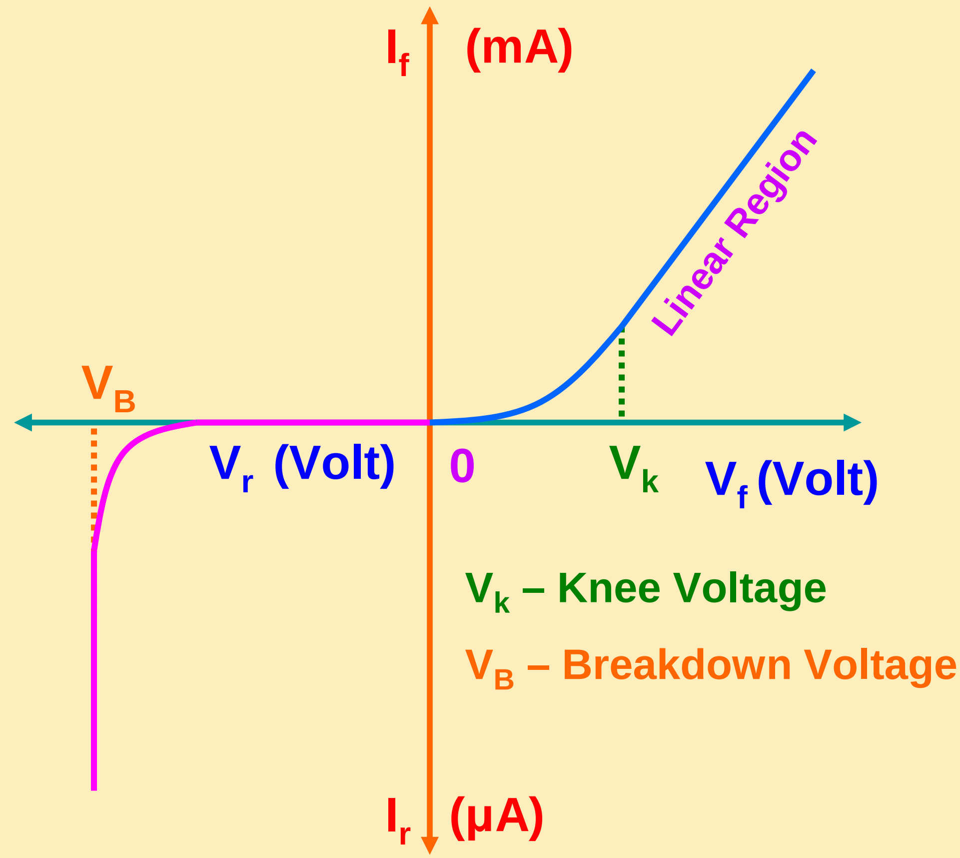
# Diode Characteristics:

## Forward Bias:




## Reverse Bias:




**Resistance of a Diode:**

i) Static or DC Resistance $\boxed{R_{d.c} = V / I}$

ii) Dynamic or AC Resistance

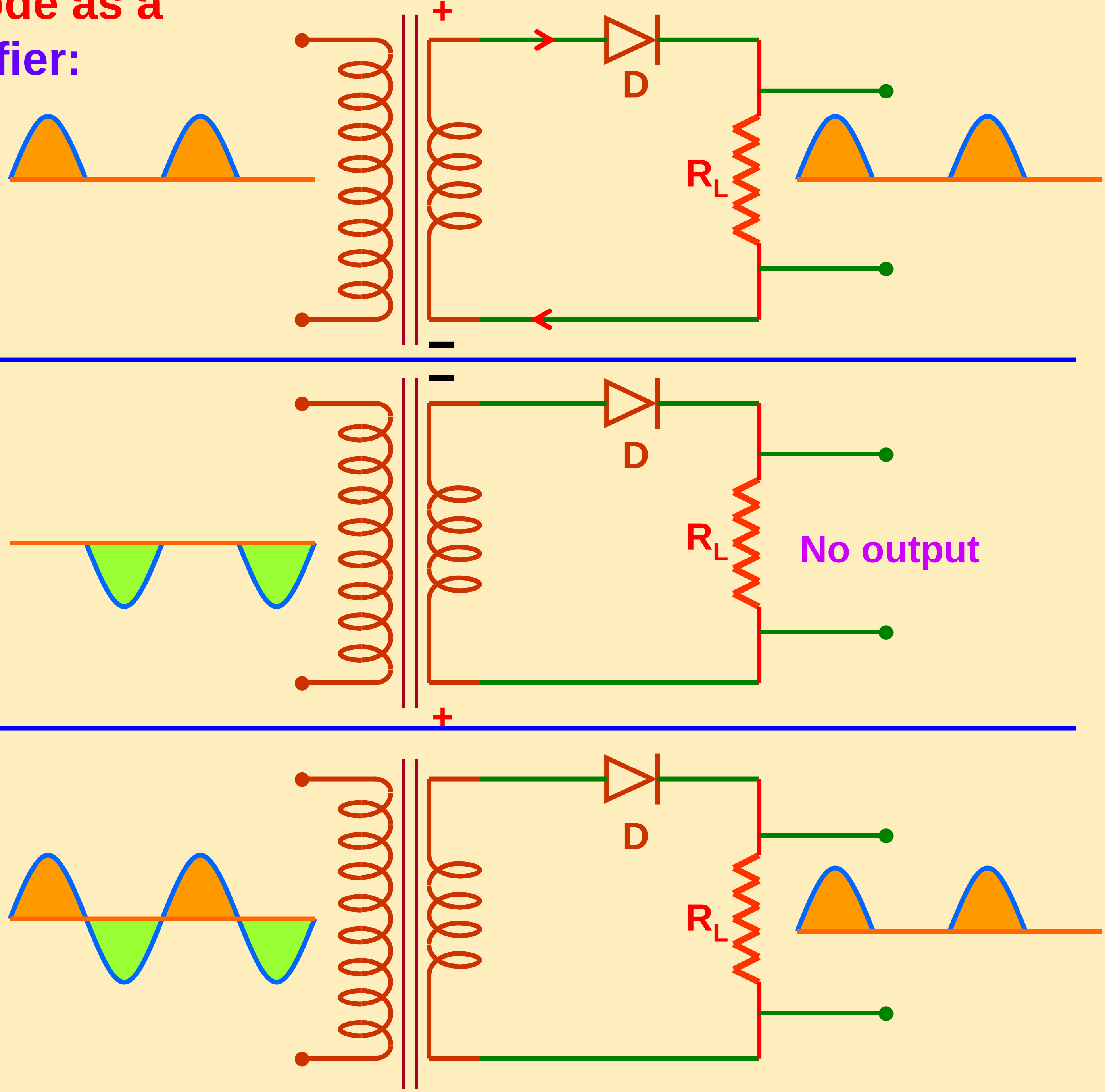
$$\boxed{R_{a.c} = \Delta V / \Delta I}$$

# PN Junction Diode as a Half Wave Rectifier:

The process of converting alternating current into direct current is called **‘rectification’.**

The device used for rectification is called **‘rectifier’.**

The PN junction diode offers low resistance in forward bias and high resistance in reverse bias.

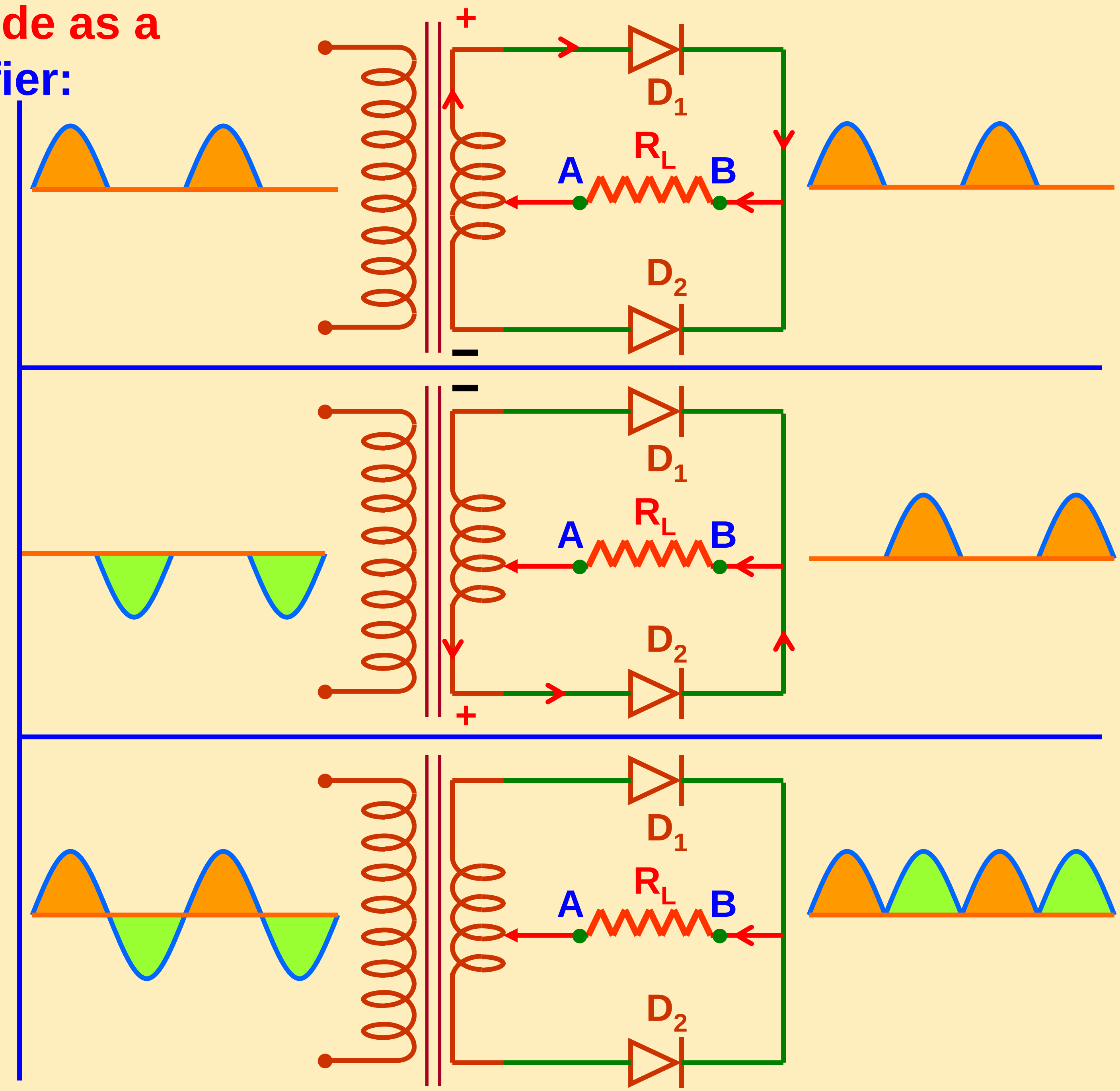


# PN Junction Diode as a Full Wave Rectifier:

When the diode rectifies whole of the AC wave, it is called **'full wave rectifier'.**

During the positive half cycle of the input ac signal, the diode $D_1$ conducts and current is through **BA**.

During the negative half cycle, the diode $D_2$ conducts and current is through **BA**.



# ELECTRONIC DEVICES - III

1. Junction Transistor
2. NPN and PNP Transistor Symbols
3. Action of NPN Transistor
4. Action of PNP Transistor
5. Transistor Characteristics in Common Base Configuration
6. Transistor Characteristics in Common Emitter Configuration
7. NPN Transistor Amplifier in Common Base Configuration
8. PNP Transistor Amplifier in Common Base Configuration
9. Various Gains in Common Base Amplifier
10. NPN Transistor Amplifier in Common Emitter Configuration
11. PNP Transistor Amplifier in Common Emitter Configuration
12. Various Gains in Common Emitter Amplifier
13. Transistor as an Oscillator

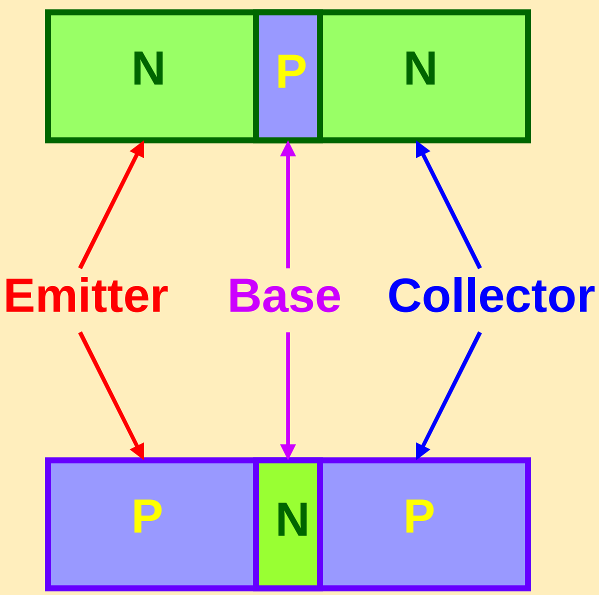
# Junction Transistor:

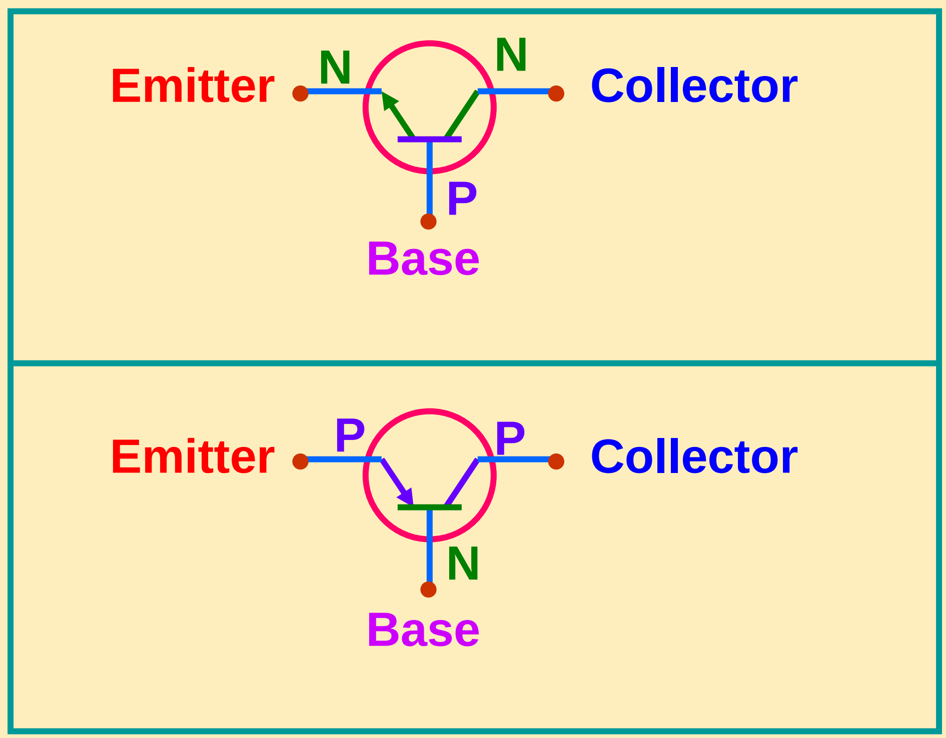
Transistor is a combination of two words 'transfer' and 'resistor' which means that transfer of resistance takes place from input to output section.

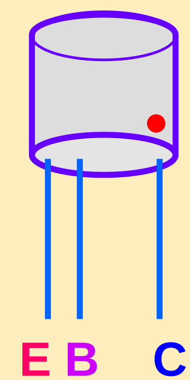
It is formed by sandwiching one type of extrinsic semiconductor between other type of extrinsic semiconductor.

NPN transistor contains P-type semiconductor sandwiched between two N-type semiconductors.

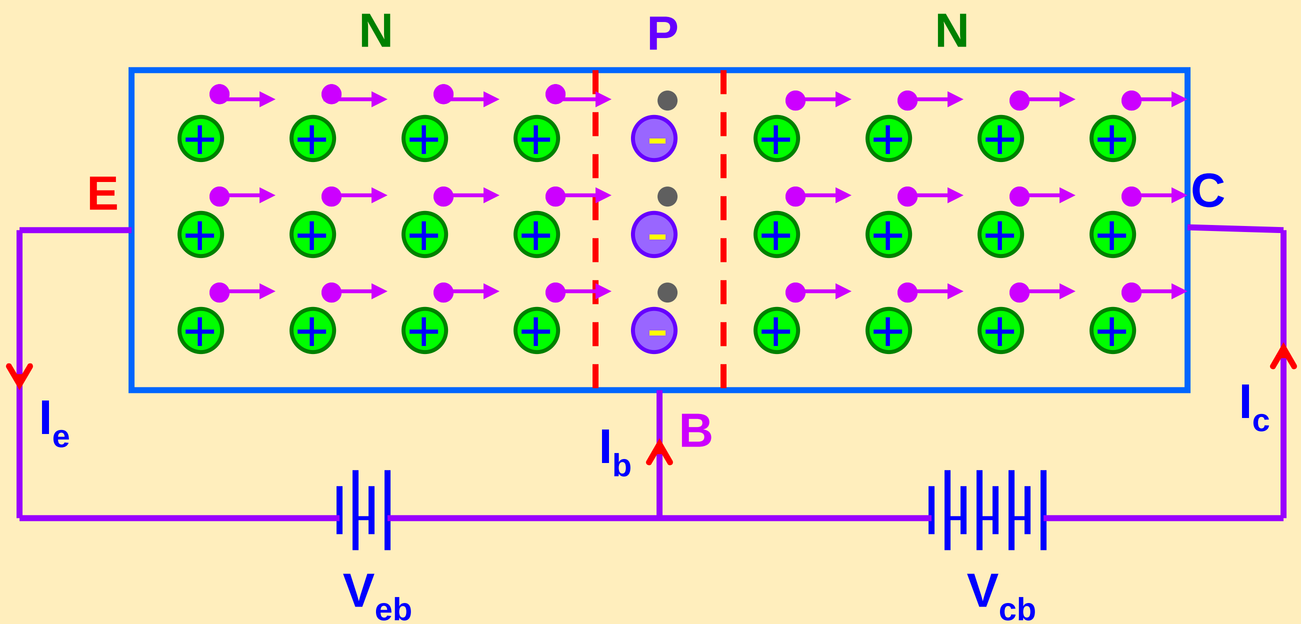
PNP transistor contains N-type semiconductor sandwiched between two P-type semiconductors.

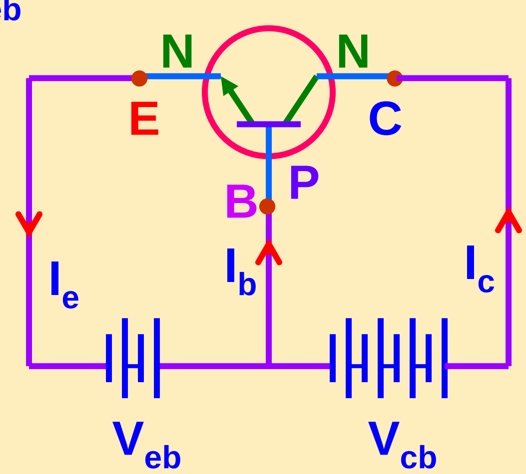


# Action of NPN Transistor:




**In NPN transistor, the arrow mark on the emitter is coming away from the base and represents the direction of flow of current. It is the direction opposite to the flow of electrons which are the main charge carriers in N-type crystal.**

**The emitter junction is forward-biased with emitter-base battery $V_{eb}$.**
**The collector junction is reverse biased with collector-base battery $V_{cb}$.**

**The forward bias of the emitter-base circuit helps the movement of electrons (majority carriers) in the emitter and holes (majority carriers) in the base towards the junction between the emitter and the base. This reduces the depletion region at this junction.**

**On the other hand, the reverse bias of the collector-base circuit forbids the movement of the majority carriers towards the collector-base junction and the depletion region increases.**

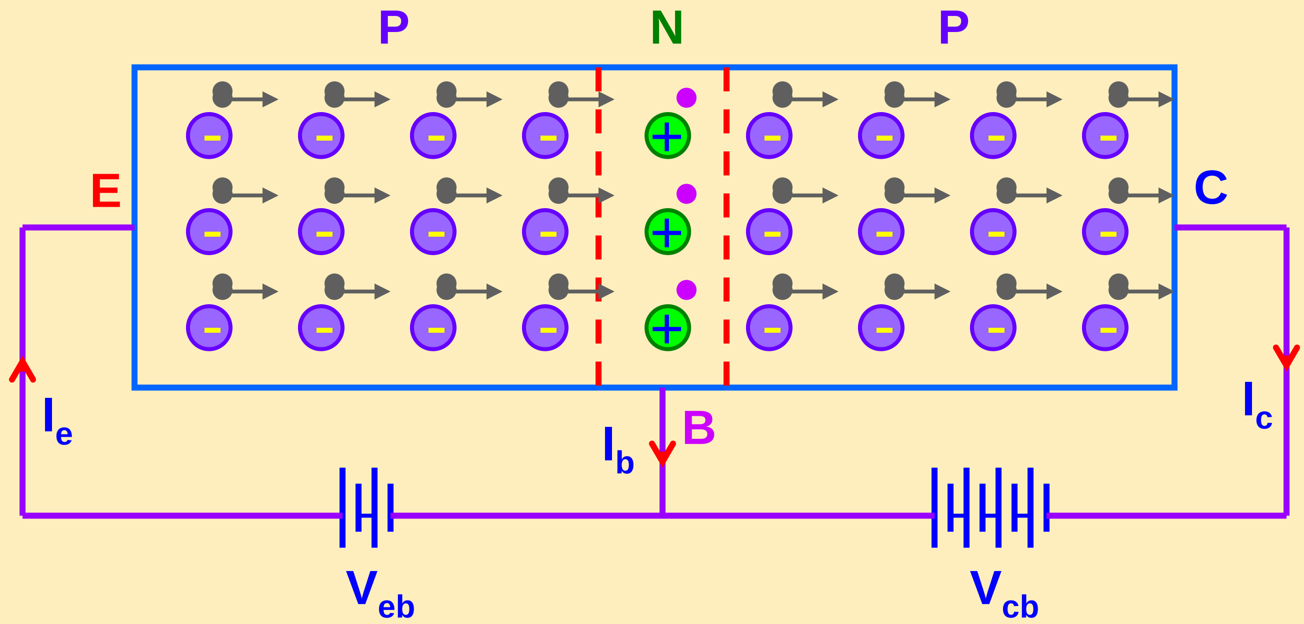
**The electrons in the emitter are repelled by the –ve terminal of the emitter-base battery. Since the base is thin and lightly doped, therefore, only a very small fraction (say, 5% ) of the incoming electrons combine with the holes. The remaining electrons rush through the collector and are swept away by the +ve terminal of the collector-base battery.**

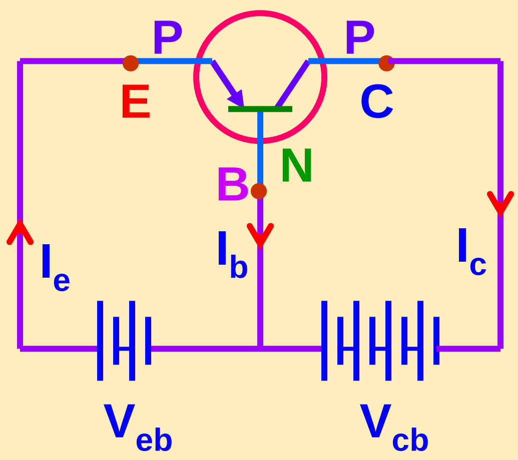
**For every electron – hole recombination that takes place at the base region one electron is released into the emitter region by the –ve terminal of the emitter-base battery. The deficiency of the electrons caused due to their movement towards the collector is also compensated by the electrons released from the emitter-base battery.**

**The current is carried by the electrons both in the external as well as inside the transistor.**

$$\boxed{I_e = I_b + I_c}$$

# Action of PNP Transistor:




**In PNP transistor, the arrow mark on the emitter is going into the base and represents the direction of flow of current. It is in the same direction as that of the movement of holes which are main charge carriers in P-type crystal.**

The emitter junction is forward-biased with emitter-base battery $V_{eb}$.
The collector junction is reverse biased with collector-base battery $V_{cb}$.

The forward bias of the emitter-base circuit helps the movement of holes (majority carriers) in the emitter and electrons (majority carriers) in the base towards the junction between the emitter and the base. This reduces the depletion region at this junction.

On the other hand, the reverse bias of the collector-base circuit forbids the movement of the majority carriers towards the collector-base junction and the depletion region increases.

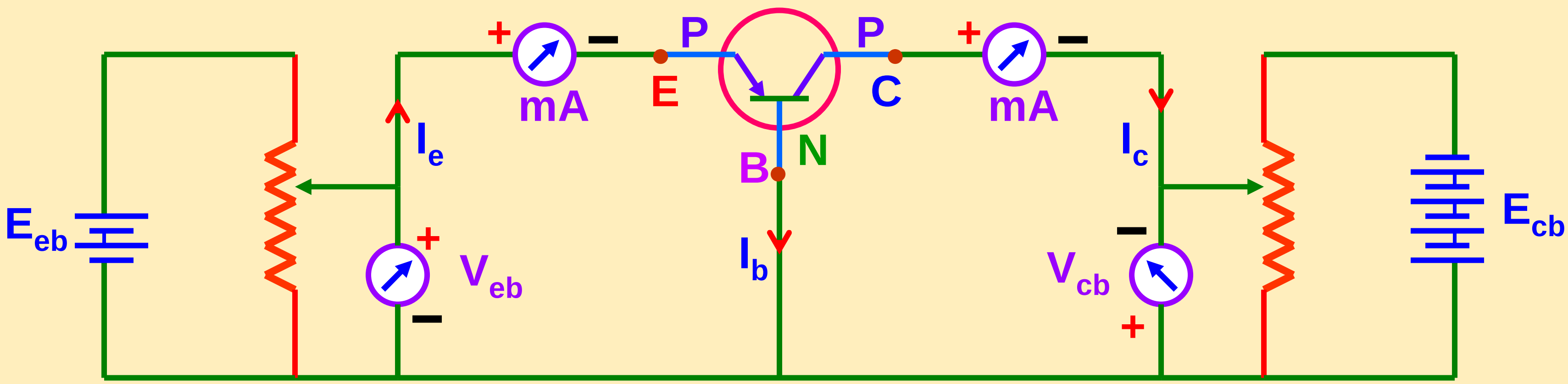
The holes in the emitter are repelled by the +ve terminal of the emitter-base battery. Since the base is thin and lightly doped, therefore, only a very small fraction (say, 5% ) of the incoming holes combine with the electrons. The remaining holes rush through the collector and are swept away by the -ve terminal of the collector-base battery.

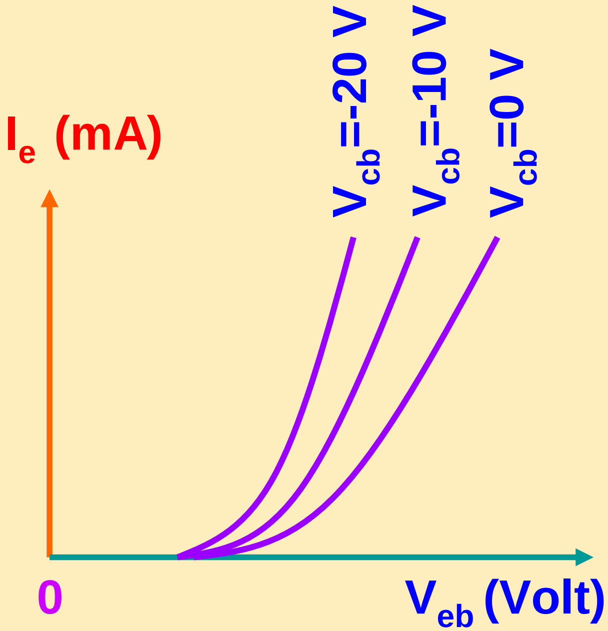
For every electron – hole recombination that takes place at the base region one electron is released into the emitter region by breaking the covalent bond and it enters the +ve terminal of the emitter-base battery. The holes reaching the collector are also compensated by the electrons released from the collector-base battery.

The current is carried by the electrons in the external circuit and by the holes inside the transistor.

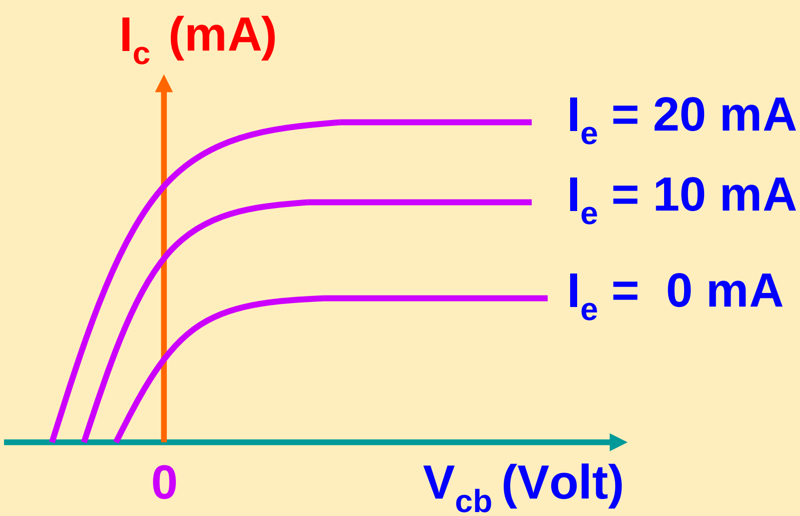
$$\boxed{I_e = I_b + I_c}$$

# PNP Transistor Characteristics in Common Base Configuration:



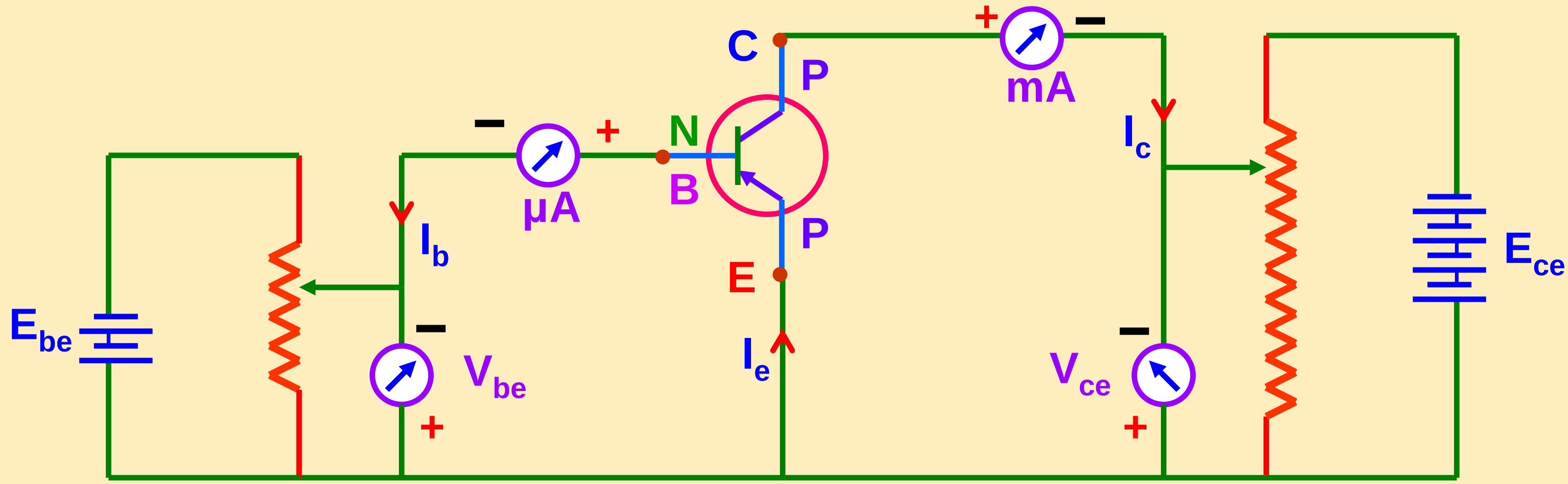



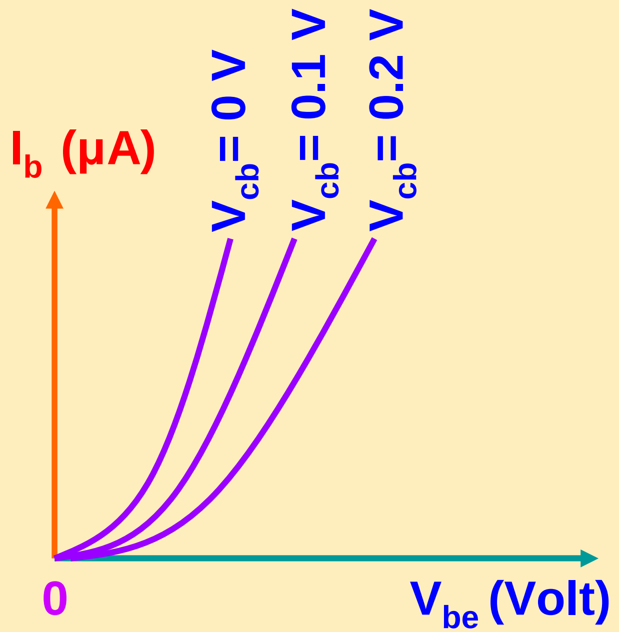

Input Characteristics



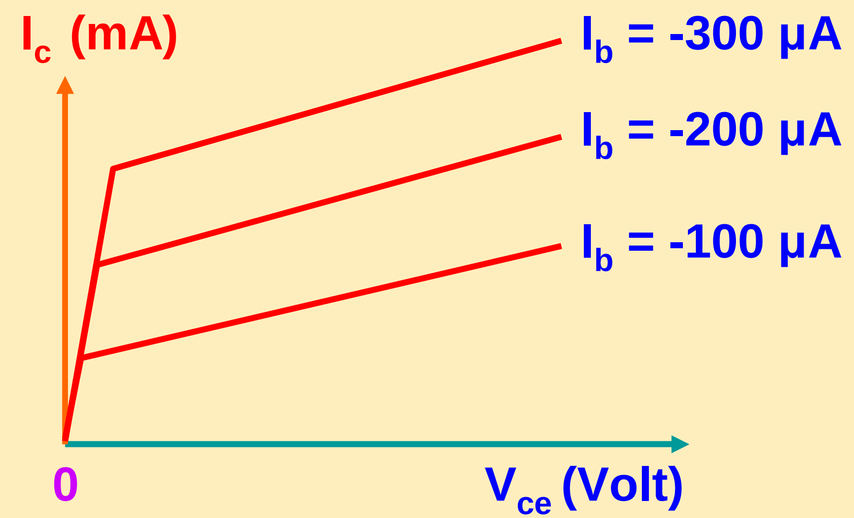

Output Characteristics

## PNP Transistor Characteristics in Common Emitter Configuration:



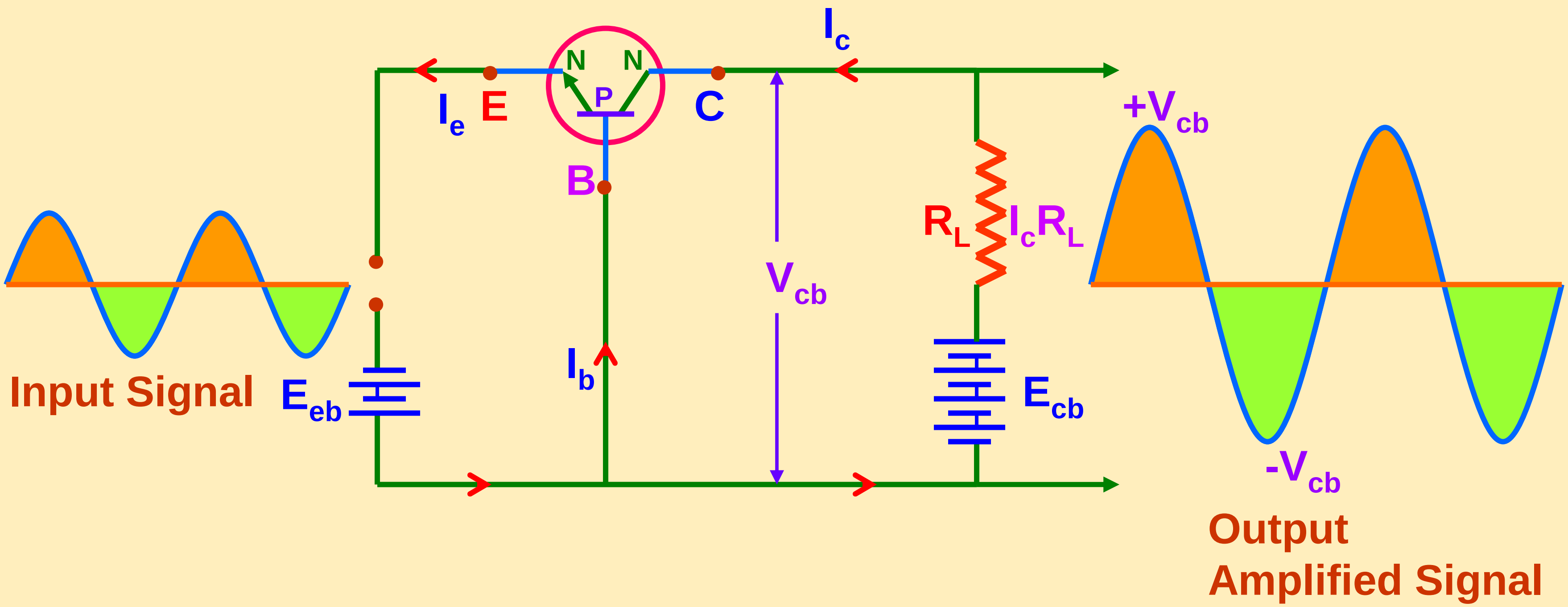




Input Characteristics




Output Characteristics

# NPN Transistor as Common Base Amplifier:




Input section is forward biased and output section is reverse biased with biasing batteries $E_{eb}$ and $E_{cb}$.

The currents $I_e$, $I_b$ and $I_c$ flow in the directions shown such that

$$I_e = I_b + I_c \text{ ……….(1)}$$

$I_cR_L$ is the potential drop across the load resistor $R_L$.

By Kirchhoff's rule,

$$V_{cb} = E_{cb} - I_c R_L \text{ ……….(2)}$$

## Phase Relation between the output and the input signal:

$V_{cb} = E_{cb} - I_c R_L$ ……….(2)

**+ve Half cycle:**

During +ve half cycle of the input sinusoidal signal, forward-bias of N-type emitter decreases (since emitter is negatively biased).

This decreases the emitter current and hence the collector current.
Base current is very small (in the order of μA).

In consequence, the voltage drop across the load resistance $R_L$ decreases.

From equation (2), it follows that $V_{cb}$ increases above the normal value.

So, the output signal is +ve for +ve input signal.

**-ve Half cycle:**

During -ve half cycle of the input sinusoidal signal, forward-bias of N-type emitter increases (since emitter is negatively biased).

This increases the emitter current and hence the collector current.
Base current is very small (in the order of μA).

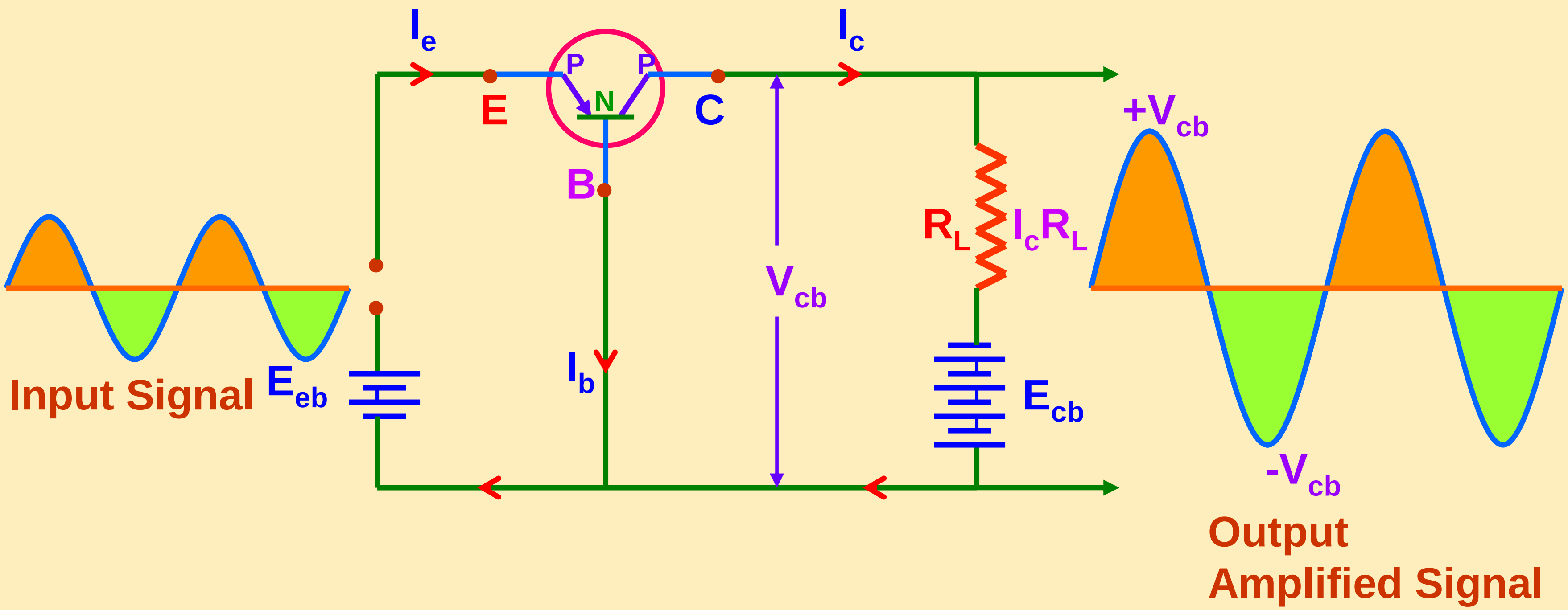
In consequence, the voltage drop across the load resistance $R_L$ increases.

From equation (2), it follows that $V_{cb}$ decreases below the normal value.

So, the output signal is -ve for -ve input signal.

Input and output are in same phase.

# PNP Transistor as Common Base Amplifier:




Input section is forward biased and output section is reverse biased with biasing batteries $E_{eb}$ and $E_{cb}$.

The currents $I_e$, $I_b$ and $I_c$ flow in the directions shown such that

$$I_e = I_b + I_c \quad ..........(1)$$

$I_cR_L$ is the potential drop across the load resistor $R_L$.

By Kirchhoff's rule,

$$V_{cb} = E_{cb} - I_c R_L \quad ..........(2)$$

## Phase Relation between the output and the input signal:

**+ve Half cycle:**

$$V_{cb} = E_{cb} - I_c R_L \quad \text{..........(2)}$$

During +ve half cycle of the input sinusoidal signal, forward-bias of P-type emitter increases (since emitter is positively biased).
This increases the emitter current and hence the collector current.
Base current is very small (in the order of μA).
In consequence, the voltage drop across the load resistance $R_L$ increases.
From equation (2), it follows that $V_{cb}$ decreases. But, since the P-type collector is negatively biased, therefore, decrease means that the collector becomes less negative w.r.t. base and the output increases above the normal value (+ve output).
So, the output signal is +ve for +ve input signal.

**-ve Half cycle:**

During -ve half cycle of the input sinusoidal signal, forward-bias of P-type emitter decreases (since emitter is positively biased).
This decreases the emitter current and hence the collector current.
Base current is very small (in the order of μA).
In consequence, the voltage drop across the load resistance $R_L$ decreases.
From equation (2), it follows that $V_{cb}$ increases. But, since the P-type collector is negatively biased, therefore, increase means that the collector becomes more negative w.r.t. base and the output decreases below the normal value (-ve output).
So, the output signal is -ve for -ve input signal.

**Input and output are in same phase.**

## Gains in Common Base Amplifier:

1) **Current Amplification Factor or Current Gain:**

(i) **DC current gain:** It is the ratio of the collector current ($I_c$) to the emitter current ($I_e$) at constant collector voltage.

$$\alpha_{dc} = \left[ \frac{I_c}{I_e} \right]_{V_{cb}}$$

(ii) **AC current gain:** It is the ratio of change in collector current ($\Delta I_c$) to the change in emitter current ($\Delta I_e$) at constant collector voltage.

$$\alpha_{ac} = \left[ \frac{\Delta I_c}{\Delta I_e} \right]_{V_{cb}}$$

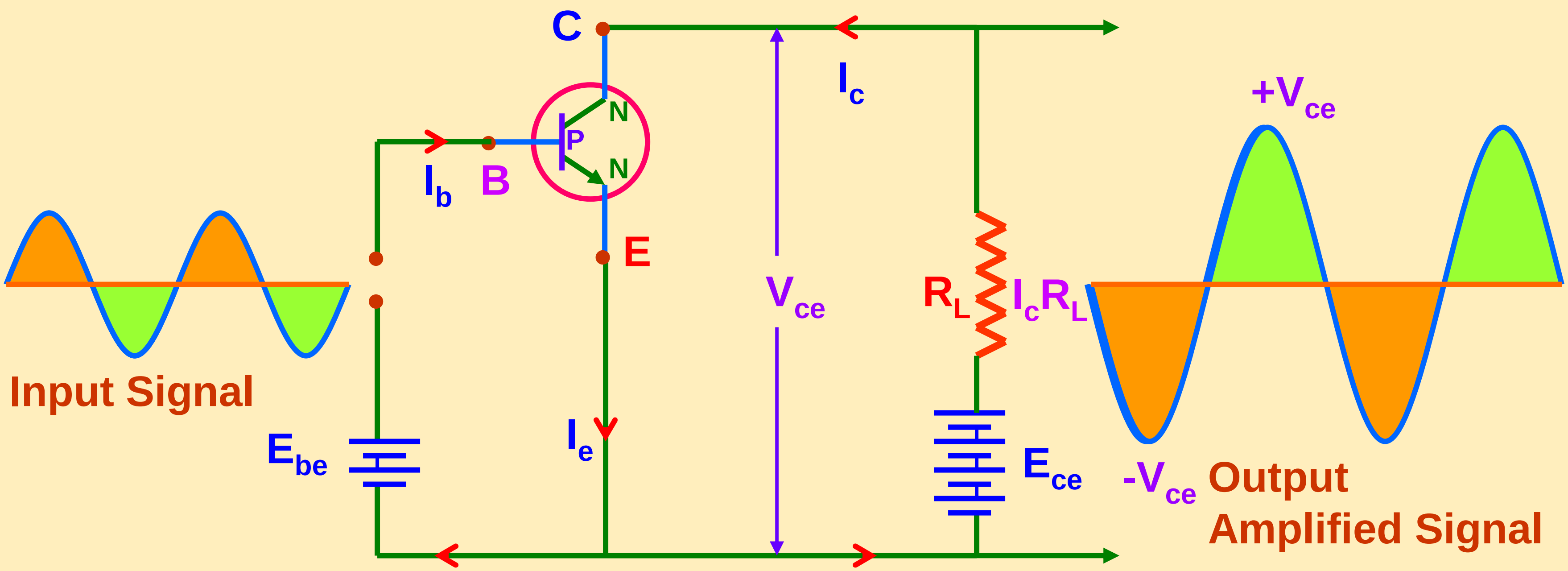
2) **AC voltage gain:** It is the ratio of change in output voltage (collector voltage $\Delta V_{cb}$) to the change in input voltage (applied signal voltage $\Delta V_i$).

$$A_{V\text{-}ac} = \left[ \frac{\Delta V_{cb}}{\Delta V_i} \right] \quad \text{or} \quad A_{V\text{-}ac} = \left[ \frac{\Delta I_c \times R_o}{\Delta I_e \times R_i} \right] \quad \text{or} \quad A_{V\text{-}ac} = \alpha_{ac} \times \text{Resistance Gain}$$

3) **AC power gain:** It is the ratio of change in output power to the change in input power.

$$A_{P\text{-}ac} = \left[ \frac{\Delta P_o}{\Delta P_i} \right] \quad \text{or} \quad A_{P\text{-}ac} = \left[ \frac{\Delta V_{cb} \times \Delta I_c}{\Delta V_i \times \Delta I_e} \right] \quad \text{or} \quad A_{P\text{-}ac} = \alpha_{ac}^2 \times \text{Resistance Gain}$$

# NPN Transistor as Common Emitter Amplifier:




Input section is forward biased and output section is reverse biased with biasing batteries $E_{be}$ and $E_{ce}$.

The currents $I_e$, $I_b$ and $I_c$ flow in the directions shown such that

$$I_e = I_b + I_c \quad \text{……….(1)}$$

$I_cR_L$ is the potential drop across the load resistor $R_L$.

By Kirchhoff's rule,

$$V_{ce} = E_{ce} - I_c R_L \quad \text{……….(2)}$$

# Phase Relation between the output and the input signal:

**+ve Half cycle:**

$$V_{ce} = E_{ce} - I_c R_L \quad \ldots\ldots\ldots(2)$$

During +ve half cycle of the input sinusoidal signal, forward-bias of base and emitter increases (since P-type base becomes more positive and N-type emitter becomes more -ve).

This increases the emitter current and hence the collector current.
Base current is very small (in the order of μA).

In consequence, the voltage drop across the load resistance $R_L$ increases.

From equation (2), it follows that $V_{ce}$ decreases below the normal value.

So, the output signal is -ve for +ve input signal.

**-ve Half cycle:**

During -ve half cycle of the input sinusoidal signal, forward-bias of P-type base and N-type emitter decreases.

This decreases the emitter current and hence the collector current.
Base current is very small (in the order of μA).

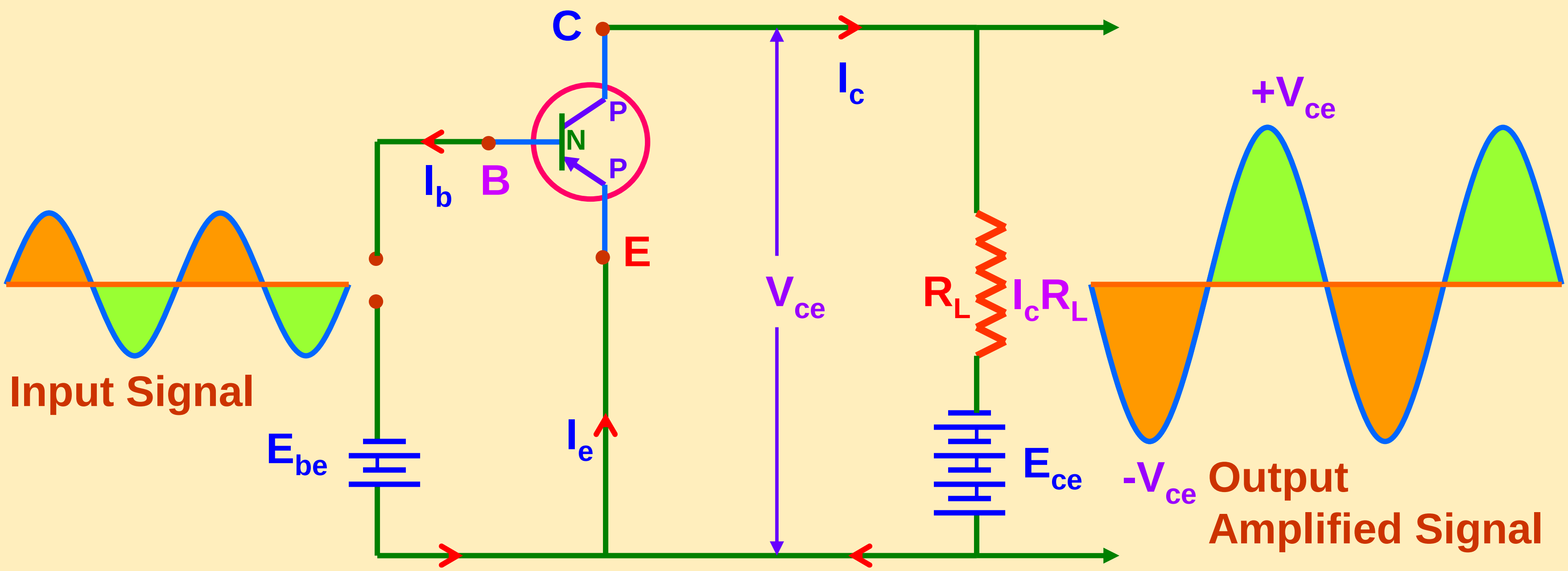
In consequence, the voltage drop across the load resistance $R_L$ decreases.

From equation (2), it follows that $V_{ce}$ increases above the normal value.

So, the output signal is +ve for -ve input signal.

Input and output are out of phase by 180°.

# PNP Transistor as Common Emitter Amplifier:




Input section is forward biased and output section is reverse biased with biasing batteries $E_{be}$ and $E_{ce}$.

The currents $I_e$, $I_b$ and $I_c$ flow in the directions shown such that

$$I_e = I_b + I_c \quad \text{……….(1)}$$

$I_cR_L$ is the potential drop across the load resistor $R_L$.

By Kirchhoff's rule,

$$V_{ce} = E_{ce} - I_c R_L \quad \text{……….(2)}$$

## Phase Relation between the output and the input signal:

**+ve Half cycle:**

$$V_{ce} = E_{ce} - I_c R_L \quad \text{..........(2)}$$

During +ve half cycle of the input sinusoidal signal, forward-bias of base and emitter decreases (since N-type base becomes less negative and P-type emitter becomes less +ve).

This decreases the emitter current and hence the collector current.

Base current is very small (in the order of μA).

In consequence, the voltage drop across the load resistance $R_L$ decreases.

From equation (2), it follows that $V_{ce}$ increases. But, since P-type collector is negatively biased, therefore, increase means that the collector becomes more negative w.r.t. base and the output goes below the normal value.

So, the output signal is -ve for +ve input signal.

**-ve Half cycle:**

During -ve half cycle of the input sinusoidal signal, forward-bias of base and emitter increases.

This increases the emitter current and hence the collector current.

Base current is very small (in the order of μA).

In consequence, the voltage drop across the load resistance $R_L$ increases.

From equation (2), it follows that $V_{ce}$ decreases. But, since P-type collector is negatively biased, therefore, decrease means that the collector becomes less negative w.r.t. base and the output goes above the normal value.

So, the output signal is +ve for -ve input signal.

**Input and output are out of phase by 180°.**

# Gains in Common Emitter Amplifier:

1) Current Amplification Factor or Current Gain:

(i) DC current gain: It is the ratio of the collector current ($I_c$) to the base current ($I_b$) at constant collector voltage.

$$\beta_{dc} = \left[ \frac{I_c}{I_b} \right]_{V_{ce}}$$

(ii) AC current gain: It is the ratio of change in collector current ($\Delta I_c$) to the change in base current ($\Delta I_b$) at constant collector voltage.

$$\beta_{ac} = \left[ \frac{\Delta I_c}{\Delta I_b} \right]_{V_{ce}}$$

2) AC voltage gain: It is the ratio of change in output voltage (collector voltage $\Delta V_{ce}$) to the change in input voltage (applied signal voltage $\Delta V_i$).

$$A_{V\text{-}ac} = \left[ \frac{\Delta V_{ce}}{\Delta V_i} \right] \quad \text{or} \quad A_{V\text{-}ac} = \left[ \frac{\Delta I_c \times R_o}{\Delta I_b \times R_i} \right] \quad \text{or} \quad A_{V\text{-}ac} = \beta_{ac} \times \text{Resistance Gain}$$

Also $A_V = g_m R_L$

3) AC power gain: It is the ratio of change in output power to the change in input power.

$$A_{P\text{-}ac} = \left[ \frac{\Delta P_o}{\Delta P_i} \right] \quad \text{or} \quad A_{P\text{-}ac} = \left[ \frac{\Delta V_{ce} \times \Delta I_c}{\Delta V_i \times \Delta I_b} \right] \quad \text{or} \quad A_{P\text{-}ac} = \beta_{ac}^2 \times \text{Resistance Gain}$$

4) **Transconductance:** It is the ratio of the small change in collector current ($\Delta I_c$) to the corresponding change in the input voltage (base voltage ($\Delta V_b$) at constant collector voltage.

$$g_m = \left[\frac{\Delta I_c}{\Delta V_b}\right]_{V_{ce}} \qquad \text{or} \qquad g_m = \frac{\beta_{ac}}{R_i}$$

## Relation between α and β:

$$I_e = I_b + I_c$$

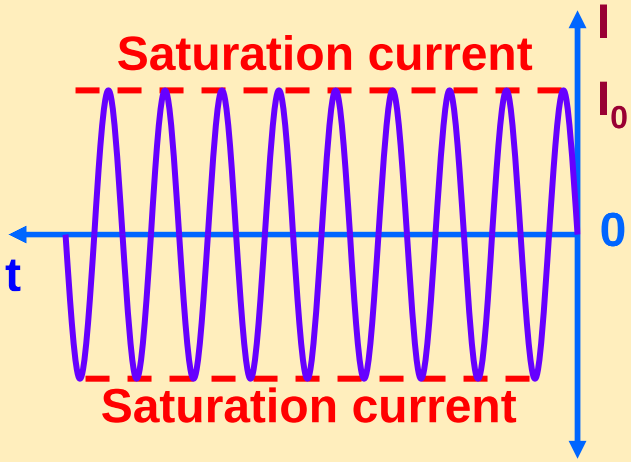
Dividing the equation by $I_c$, we get

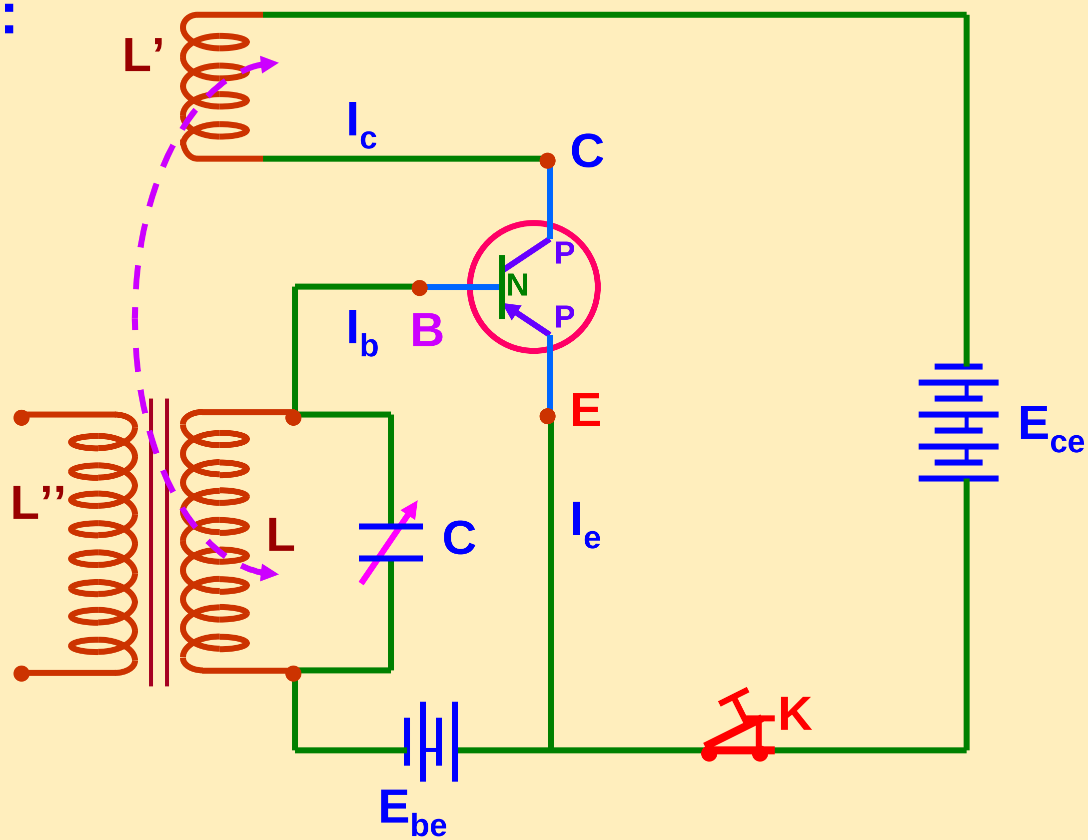
$$\frac{I_e}{I_c} = \frac{I_b}{I_c} + 1$$

But $\quad \alpha = \left[\frac{I_c}{I_e}\right] \quad$ and $\quad \beta = \left[\frac{I_c}{I_b}\right]$

$$\therefore \quad \frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \text{or} \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \quad \text{and} \quad \boxed{\alpha = \frac{\beta}{1+\beta}}$$

# Transistor as an Oscillator:
# (PNP)




An oscillator is a device which can produce undamped electromagnetic oscillations of desired frequency and amplitude.

It is a device which delivers a.c. output waveform of desired frequency from d.c. power even without input signal excitation.

Tank circuit containing an inductance L and a capacitance C connected in parallel can oscillate the energy given to it between electrostatic and magnetic energies. However, the oscillations die away since the amplitude decreases rapidly due to inherent electrical resistance in the circuit.

In order to obtain undamped oscillations of constant amplitude, transistor can be used to give regenerative or positive feedback from the output circuit to the input circuit so that the circuit losses can be compensated.

When key K is closed, collector current begins to grow through the tickler coil L' . Magnetic flux linked with L' as well as L increases as they are inductively coupled. Due to change in magnetic flux, induced emf is set up in such a direction that the emitter – base junction is forward biased. This increases the emitter current and hence the collector current.

With the increase in collector current , the magnetic flux across L' and L increases. The process continues till the collector current reaches the saturation value. During this process the upper plate of the capacitor C gets positively charged.

At this stage, induced emf in L becomes zero. The capacitor C starts discharging through the inductor L.

The emitter current starts decreasing resulting in the decrease in collector current. Again the magnetic flux changes in L' and L but it induces emf in such a direction that it decreases the forward bias of emitter – base junction.

As a result, emitter current further decreases and hence collector current also decreases. This continues till the collector current becomes zero. At this stage, the magnetic flux linked with the coils become zero and hence no induced emf across L.

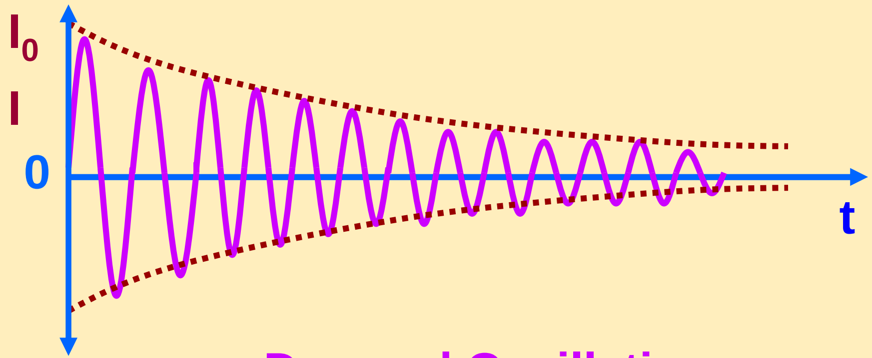
However, the decreasing current after reaching zero value overshoots (goes below zero) and hence the current starts increasing but in the opposite direction. During this period, the lower plate of the capacitor C gets +vely charged.

This process continues till the current reaches the saturation value in the negative direction. At this stage, the capacitor starts discharging but in the opposite direction (giving positive feedback) and the current reaches zero value from –ve value.

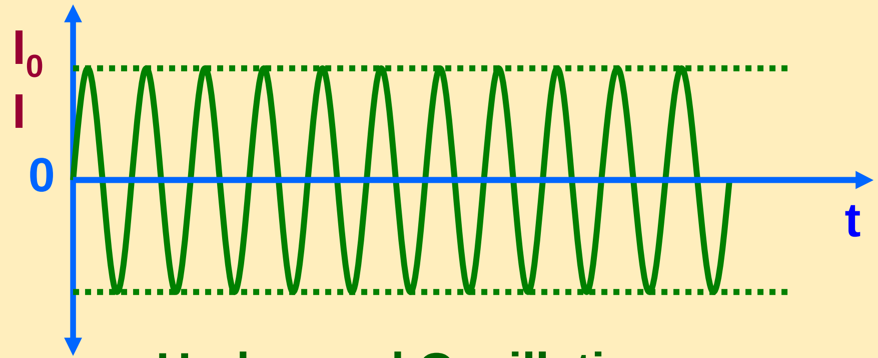
The cycle again repeats and hence the oscillations are produced.
The output is obtained across L''.

The frequency of oscillations is given by

$$\boxed{f = \frac{1}{2\pi\sqrt{LC}}}$$



Damped Oscillations

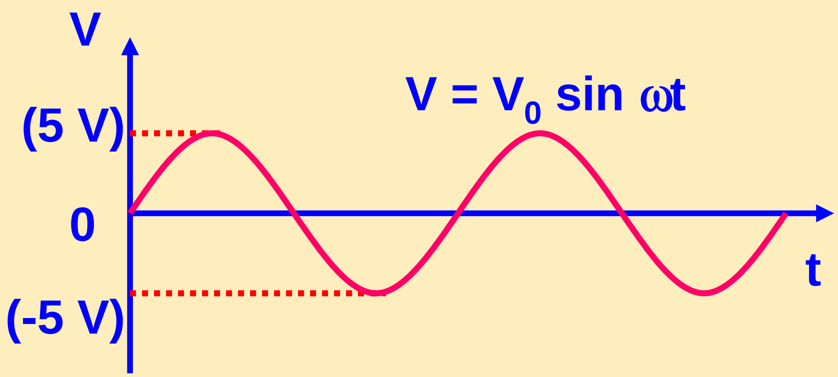


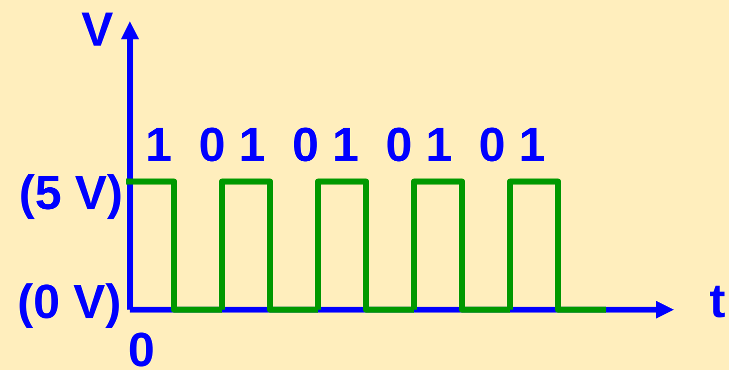
Undamped Oscillations

# ELECTRONIC DEVICES - IV

1. Analog and Digital Signal
2. Binary Number System
3. Binary Equivalence of Decimal Numbers
4. Boolean Algebra
5. Logic Operations: OR, AND and NOT
6. Electrical Circuits for OR, AND and NOT Operations
7. Logic Gates and Truth Table
8. Fundamental Logic Gates: OR, AND and NOT (Digital Circuits)
9. NOR and NAND Gates
10. NOR Gate as a Building Block
11. NAND Gate as a Building Block
12. XOR Gate

| Analogue signal | Digital signal |
|---|---|
| A continuous signal value which at any instant lies within the range of a maximum and a minimum value. | A discontinuous signal value which appears in steps in pre-determined levels rather than having the continuous change. |




**Digital Circuit:**

An electrical or electronic circuit which operates only in two states (binary mode) namely ON and OFF is called a Digital Circuit.

In digital system, high value of voltage such as +10 V or +5 V is represented by ON state or 1 (state) whereas low value of voltage such as 0 V or -5V or -10 V is represented by OFF state or 0 (state).

## Binary Number System:

A number system which has only two digits i.e. 0 and 1 is known as binary number system or binary system.

The states ON and OFF are represented by the digits 1 and 0 respectively in the binary number system.

## Binary Equivalence of Decimal Numbers:

Decimal number system has base (or radix) 10 because of 10 digits viz. 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9 used in the system.

Binary number system has base (or radix) 2 because of 2 digits viz. 0 and 2 used in the system.

| D | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|
| B | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 |

| D | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|
| B | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |

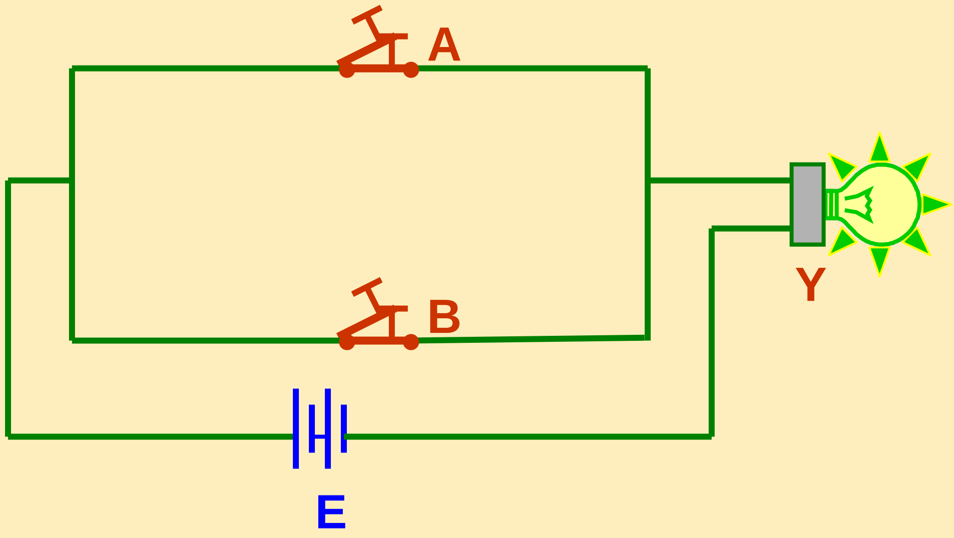
## Boolean Algebra:

George Boole developed an algebra called Boolean Algebra to solve logical problems. In this, 3 logical operations viz. OR, AND and NOT are performed on the variables.

The two values or states represent either 'TRUE' or 'FALSE'; 'ON' or 'OFF'; 'HIGH' or 'LOW'; 'CLOSED' or 'OPEN'; 1 or 0 respectively.

## OR Operation:

OR operation is represented by '+'.
Its boolean expression is Y = A + B
It is read as "Y equals A OR B".
It means that "if A is true OR B is true, then Y will be true".

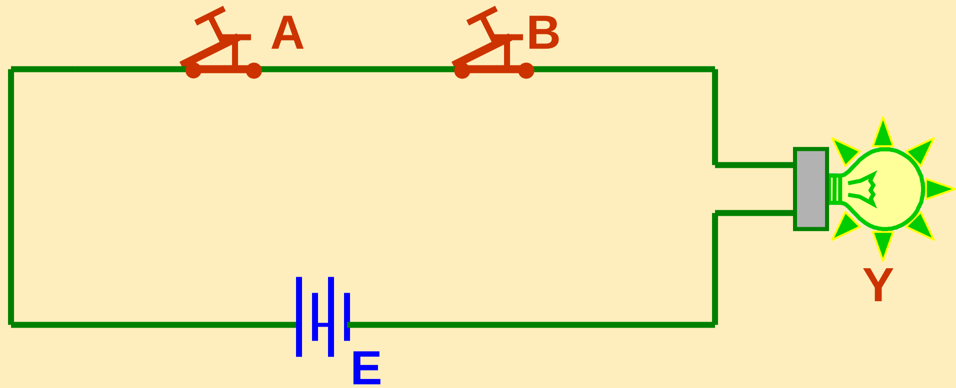



**Truth Table**

| Switch A | Switch B | Bulb Y |
|---|---|---|
| OFF | OFF | OFF |
| OFF | ON | ON |
| ON | OFF | ON |
| ON | ON | ON |

## AND Operation:

AND operation is represented by '.'
Its boolean expression is $Y = A . B$
It is read as "Y equals A AND B".
It means that "if both A and B are true, then Y will be true".

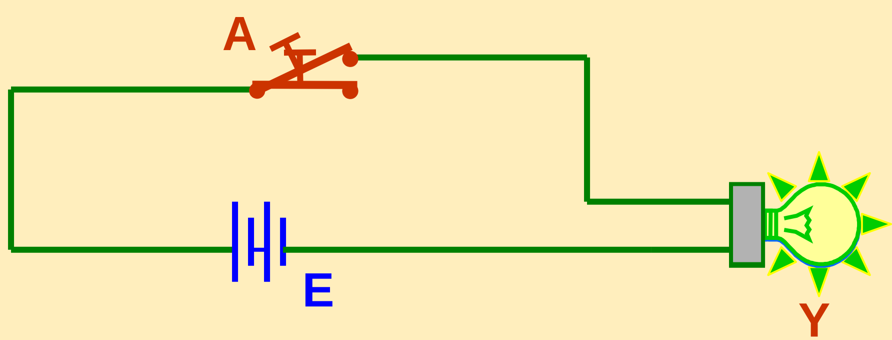



Truth Table

| Switch A | Switch B | Bulb Y |
|---|---|---|
| OFF | OFF | OFF |
| OFF | ON | OFF |
| ON | OFF | OFF |
| ON | ON | ON |

## NOT Operation:

NOT operation is represented by ′ or ¯ .Its boolean expression is $Y = A'$ or $\bar{A}$
It is read as "Y equals NOT A". It means that "if A is true, then Y will be false".




Truth Table

| Switch A | Bulb Y |
|---|---|
| OFF | ON |
| ON | OFF |

## Logic Gates:

The digital circuit that can be analysed with the help of Boolean Algebra is called logic gate or logic circuit.

A logic gate can have two or more inputs but only one output.

There are 3 fundamental logic gates namely OR gate, AND gate and NOT gate.

## Truth Table:

The operation of a logic gate or circuit can be represented in a table which contains all possible inputs and their corresponding outputs is called a truth table.

If there are n inputs in any logic gate, then there will be $n^2$ possible input combinations.

0 and 1 inputs are taken in the order of ascending binary numbers for easy understanding and analysis.

### Eg. for 4 input gate

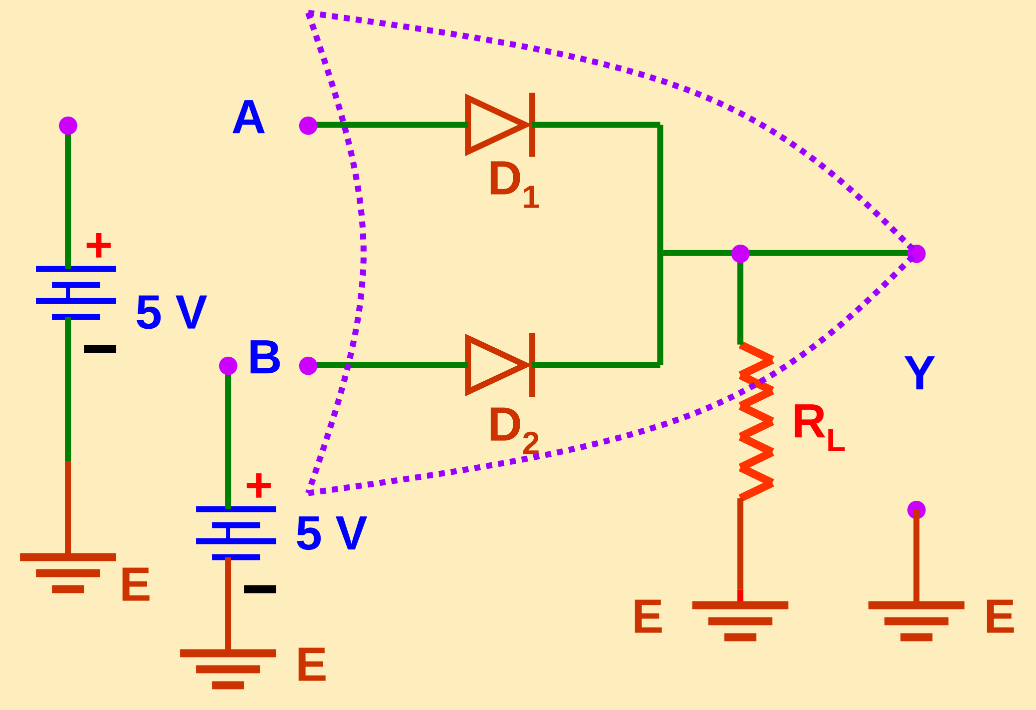
| A | B | C | D |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |

# Digital OR Gate:

The positive voltage (+5 V) corresponds to high input i.e. 1 (state).

The negative terminal of the battery is grounded and corresponds to low input i.e. 0 (state).

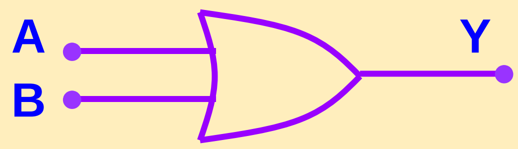
Case 1: Both A and B are given 0 input and the diodes do not conduct current. Hence no output is across $R_L$. i.e. Y = 0




Case 2: A is given 0 and B is given 1. Diode $D_1$ does not conduct current (cut-off) but $D_2$ conducts. Hence output (5 V) is available across $R_L$. i.e. Y = 1

Case 3: A is given 1 and B is given 0. Diode $D_1$ conducts current but $D_2$ does not conduct. Hence output (5 V) is available across $R_L$. i.e. Y = 1

Case 4: A and B are given 1. Both the diodes conduct current. However output (only 5 V) is available across $R_L$. i.e. Y = 1



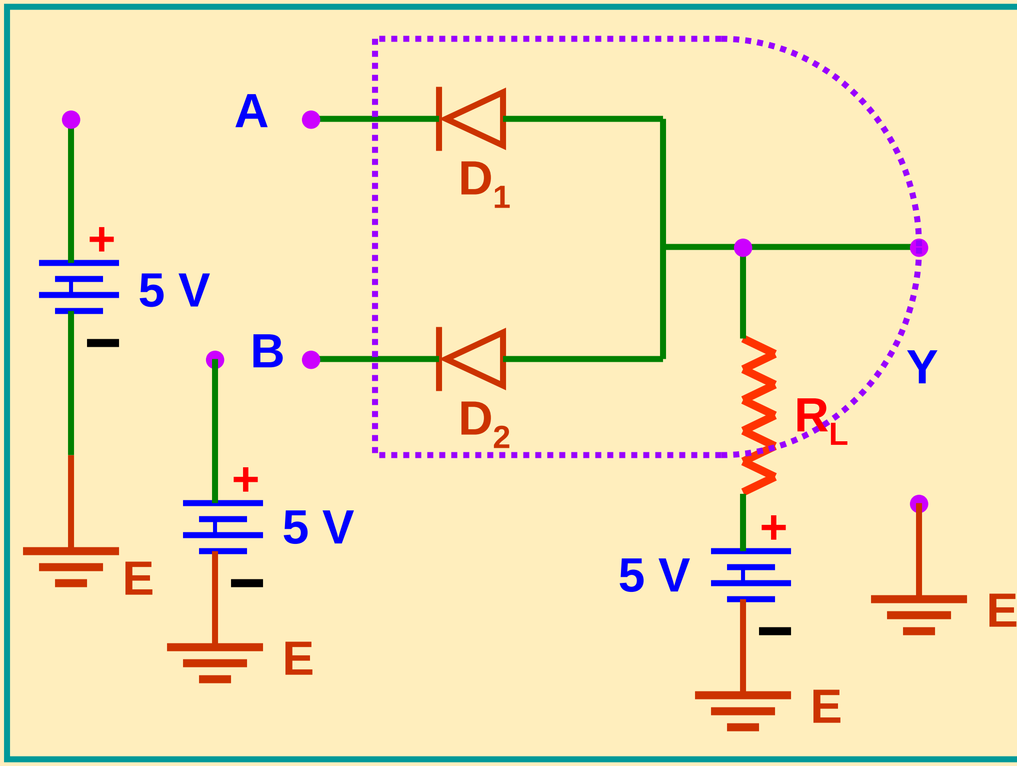

Truth Table

| A | B | Y = A + B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

# Digital AND Gate:

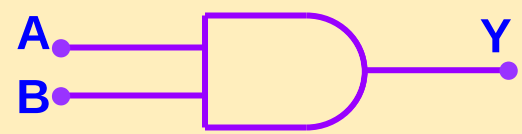
**Case 1:** Both A and B are given 0 input and the diodes conduct current (Forward biased). Since the current is drained to the earth, hence, no output across $R_L$.
i.e. Y = 0

**Case 2:** A is given 0 and B is given 1. Diode $D_1$ being forward biased conducts current but $D_2$ does not conduct. However, the current from the output battery is drained through $D_1$. So, Y = 0




**Case 3:** A is given 1 and B is given 0. Diode $D_1$ does not conduct current but $D_2$ being forward biased conducts . However, the current from the output battery is drained through $D_2$. Hence, no output is available across $R_L$. i.e. Y = 0

**Case 4:** A and B are given 1. Both the diodes do not conduct current. The current from the output battery is available across $R_L$ and output circuit. Hence, there is voltage drop (5 V) across $R_L$. i.e. Y = 1



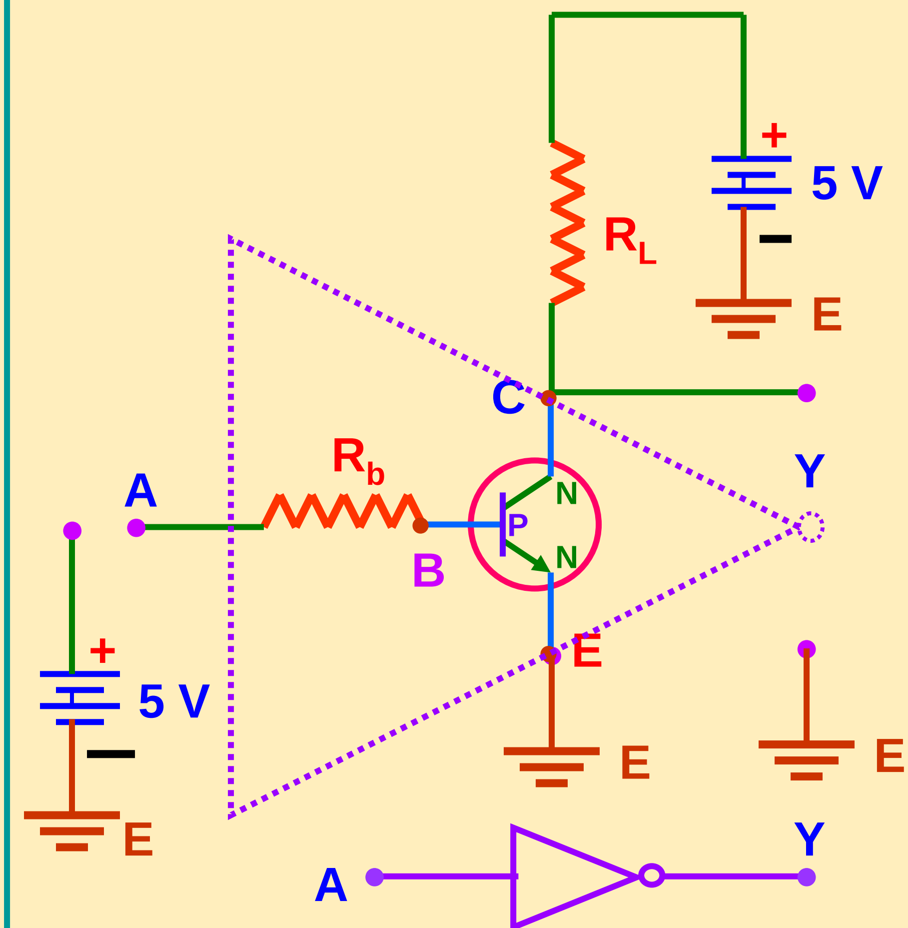

Truth Table

| A | B | Y = A . B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

# Digital NOT Gate:

NPN transistor is connected to biasing batteries through Base resistor ($R_b$) and Collector resistor ($R_L$). Emitter is directly earthed. Input is given through the base and the output is tapped across the collector.

Case 1: A is given 0 input. In the absence of forward bias to the P-type base and N-type emitter, the transistor is in cut-off mode (does not conduct current). Hence, the current from the collector battery is available across the output unit. Therefore, voltage drop of 5 V is available across Y. i.e. Y= 1



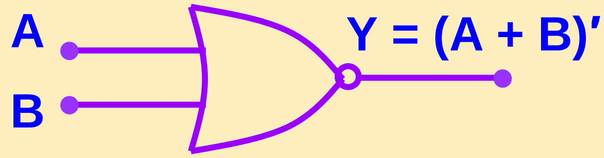

Case 2: A is given 1 input by connecting the +ve terminal of the input battery. P-type base being forward biased makes the transistor in conduction mode. The current supplied by the collector battery is drained through the transistor to the earth. Therefore, no output is available across Y. i.e. Y = 0

Truth Table

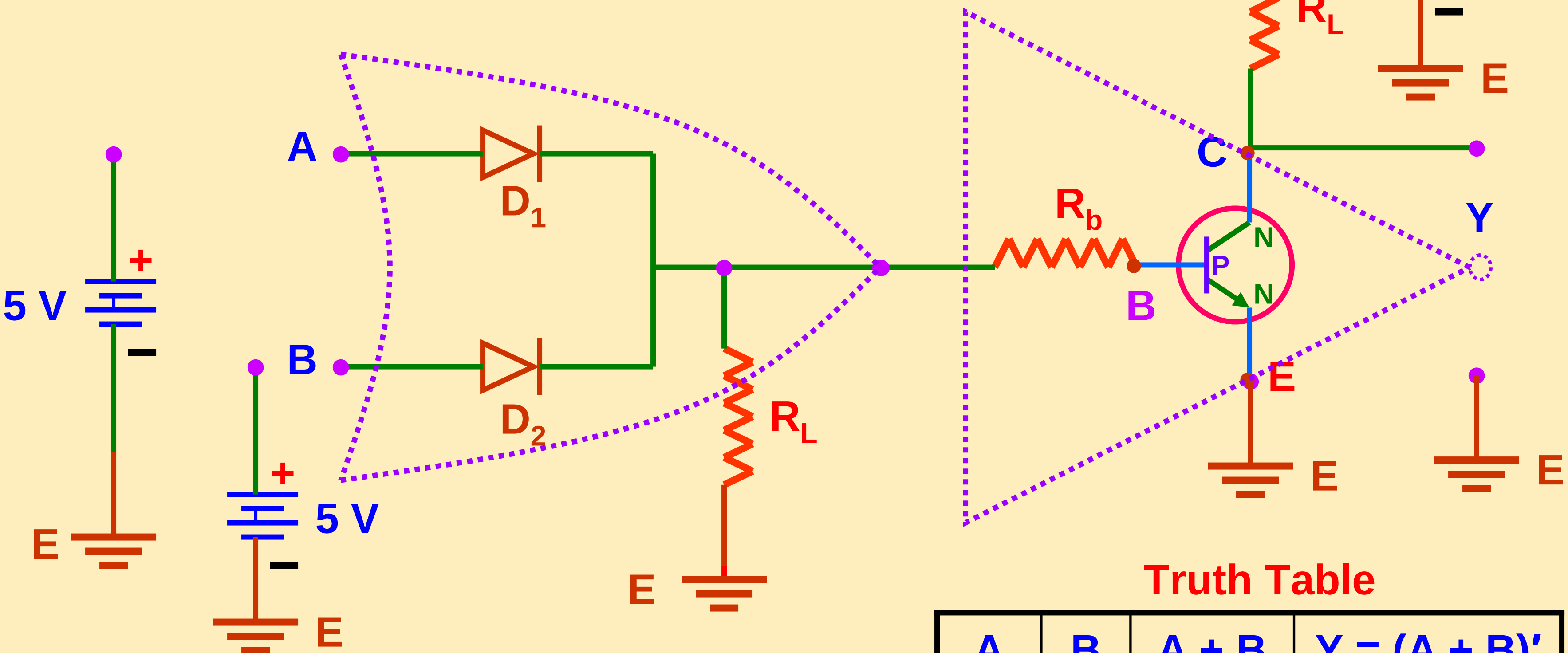
| A | Y=A′ |
|---|---|
| 0 | 1 |
| 1 | 0 |

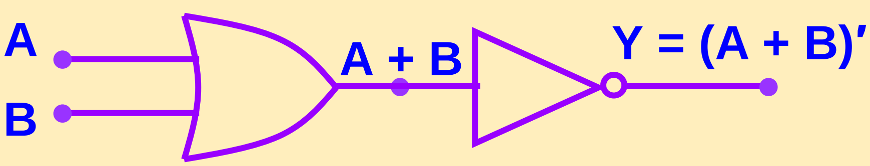
# NOR Gate:

## Symbol:




## Circuit:



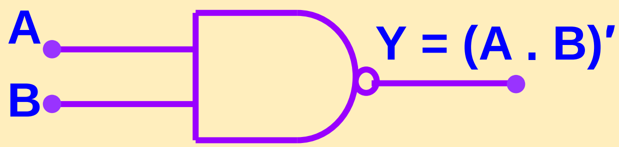




**Truth Table**

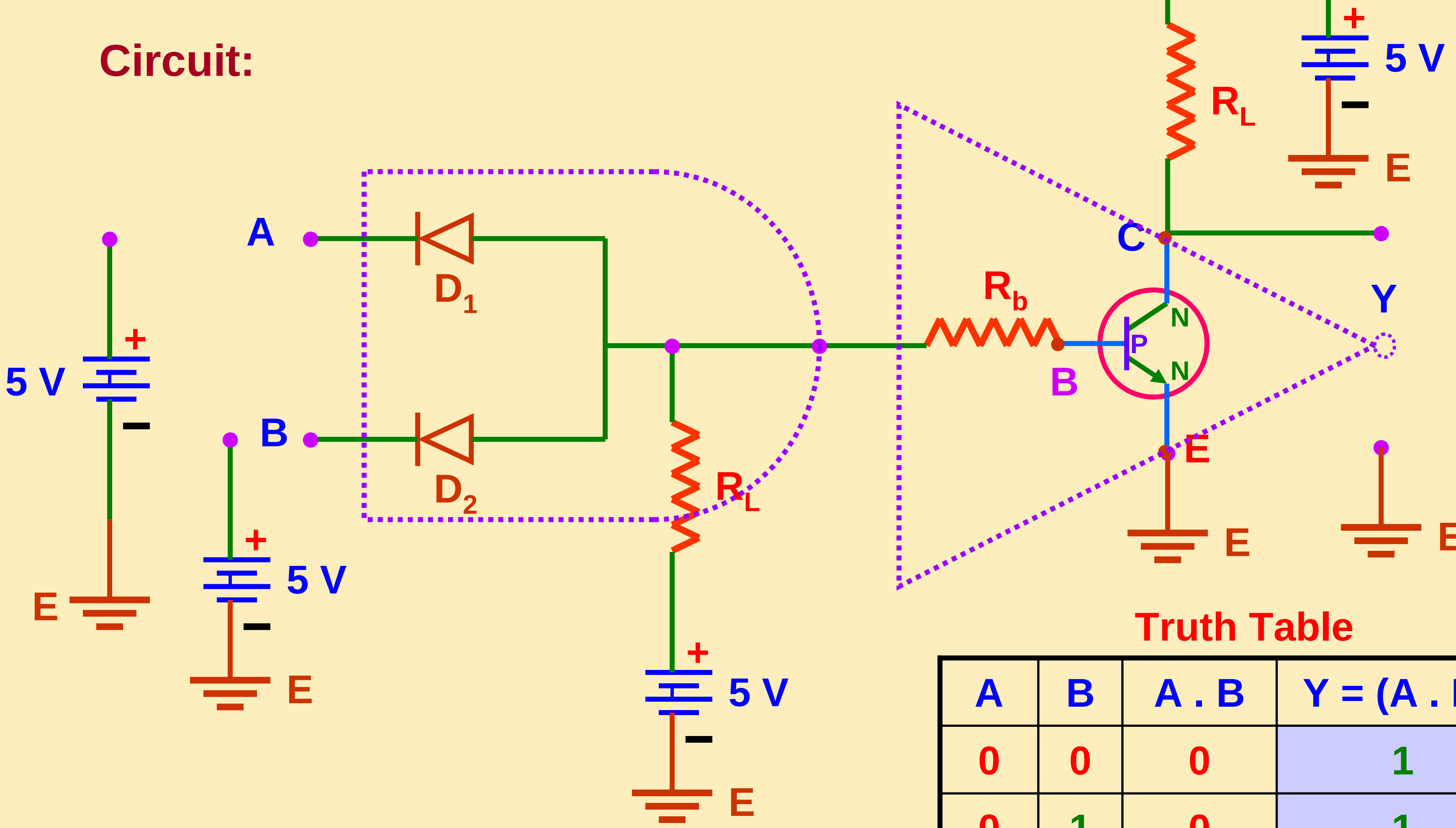
| A | B | A + B | Y = (A + B)′ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

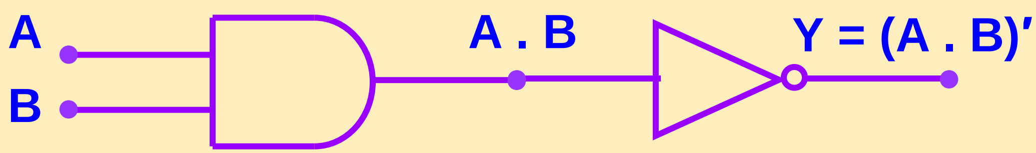
## NAND Gate:

### Symbol:




### Circuit:



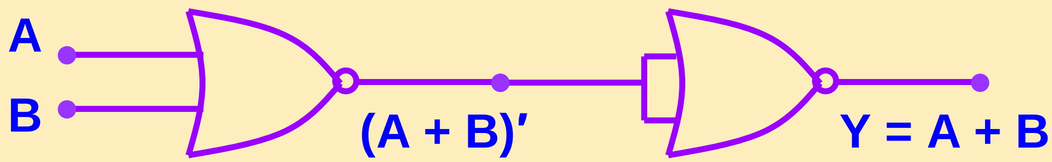




**Truth Table**

| A | B | A . B | Y = (A . B)′ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

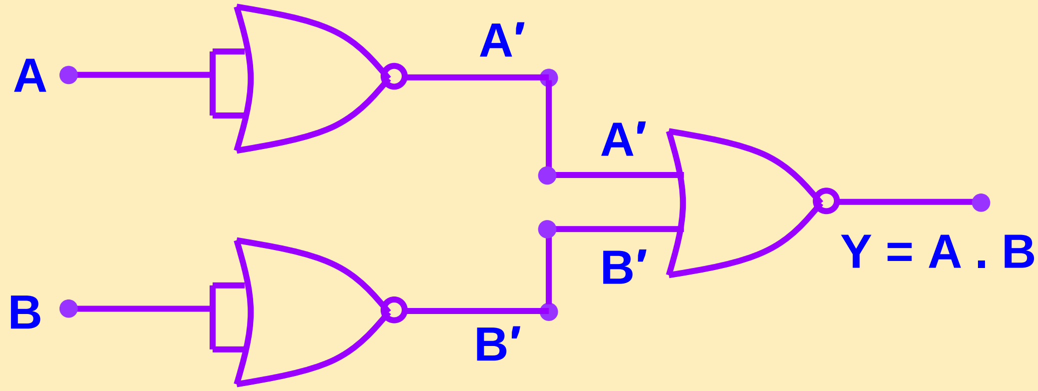
# NOR Gate as a Building Block:

## OR Gate:



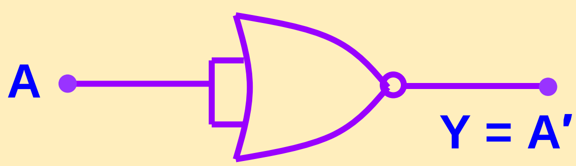

| A | B | (A + B)′ | A + B |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |

## AND Gate:




| A | B | A′ | B′ | A′+B′ | (A′+B′)′ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

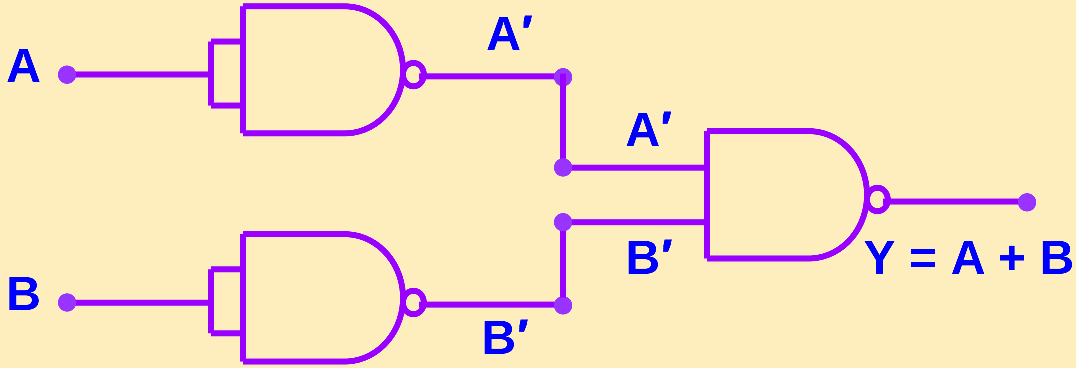
## NOT Gate:




| A | A′ |
|---|---|
| 0 | 1 |
| 1 | 0 |

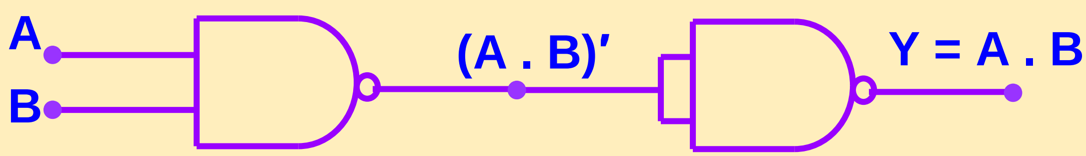
# NAND Gate as a Building Block:

## OR Gate:



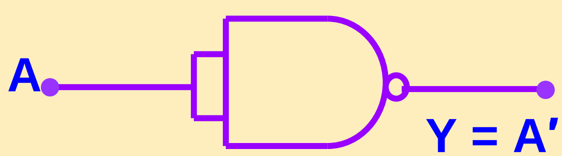

| A | B | A′ | B′ | A′.B′ | (A′ . B′)′ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |

## AND Gate:



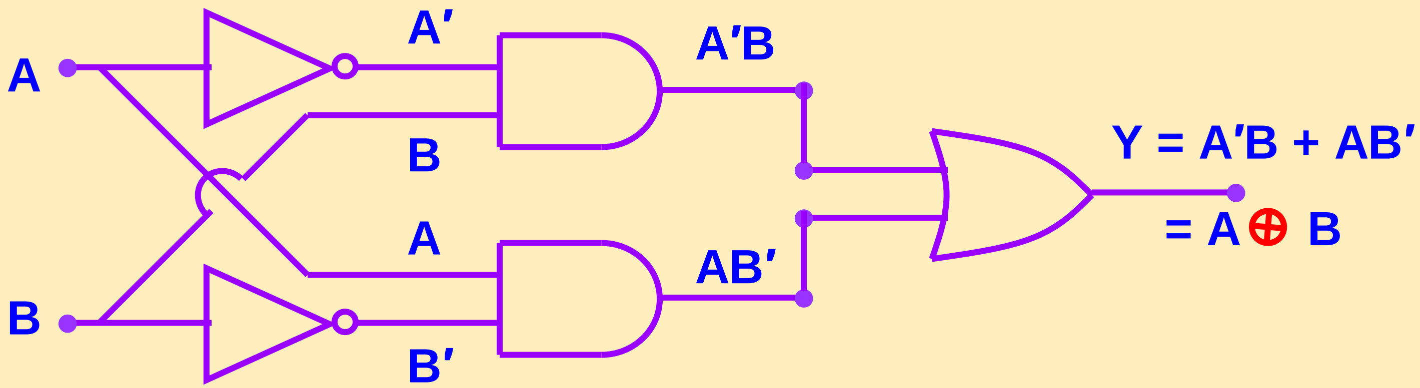

| A | B | (A . B)′ | A . B |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

## NOT Gate:




| A | A′ |
|---|---|
| 0 | 1 |
| 1 | 0 |

# XOR Gate:




| A | B | A′ | B′ | A′B | AB′ | Y = A′B + AB′ = A ⊕ B |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |