## B.TECH. DEGREE III SEMESTER (SUPPLEMENTARY) EXAMINATION IN INFORMATION TECHNOLOGY/COMPUTER SCIENCE AND ENGINEERING JUNE 2001

## IT/CS 304 DIGITAL CIRCUITS AND LOGIC DESIGN

(1995 Admissions)

Time: 3 Hours

Maximum Marks: 100

- 1. Answer all questions.
- 2. All Questions carry equal marks.

1.	a.	State and prove the Distributive laws of Boolean Algebra	10
	b	Prove the following:	10
		(i) $A + AB = A$ , (ii) $A + A'B = A + B$ (iii) $AB + AB' = A$	
		OR	
11.	<b>a</b> .	<ul> <li>(i) Find the decimal number whose binary representation is 10011</li> <li>(ii) Convert the decimal number 1.8125 to binary</li> <li>(iii) Represent the decimal numbers 0, 1, 2, and 3 in the Grey Reflected binary code</li> </ul>	3 3 . 4
	b.	Given the logical function of five variables, $f(a,b,c,d,e) = [a+(bc)'](d+be)'$ express the function as a sum of products.	10
III.	a.	Use Karnaugh map to reduce the following function	8
		f = ABC'D' + AB'C'D' + (AB)'CD + A'B'CD' + AB'CD'	
	b.	Minimize the following expression using Karnaugh map method: (i) $\sum m(0, 1, 2, 3, 4, 5, 9, 10, 12, 13, 14, 15)$ (ii) $BC' + A'B + A'B'D' + BCD + AB'C'D'$ OR	6 6
IV.	a.	Using a minimum number of two-input NAND gates, design a logic circuit to realize the logic function $Y = \sum m(0, 1, 2, 3, 8, 9, 10, 11)$	10
	b.	With the help of input-output characteristics of an inverter, discuss what is meant by noise-margin	10



		2	
V.	a.	Explain tristate logic	10
	b.	How is TTL logic interfaced to CMOS logic?	10
		OR	
V <sub>i</sub> L.	a.	Draw the circuit of a TTL NAND gate with active pull-up, and discuss the operation of the circuit. How is the circuit modified to have a tristate output?	10
	b.	Design a CMOS circuit to realize the logic function $Y = (AB + C)'$	10
VII.	<b>a</b> .	Design a circuit with JK F/Fs and two input NAND gates that count the sequence 000, 001, 100, 101, 111, 000,	. 10
	<b>b</b> .	Draw the circuit of a 4-bit shift register with a mode control input, M. When $M = 0$ , $4 - bits$ of data are loaded into the shift register and when $M = 1$ , data is shifted to the right, with "1" being loaded in the leftmost bit.	10
		OR	
VIII.	a.	Draw the circuit of a binary up/down converter and explain its operation	10
	b.	Compare the features of TTL and ECL logic families.	10
IX.	a.	Explain the basic structure and operation of an EPROM	10
	b.	Write short notes on the following:	10
		(i) VLSI (ii) MOSFET	
		OR	
X.	a.	Explain the advantages and disadvantages of programmed logic	10
	b.	Write short notes on the following:	10
		(i) BJT RAM cell (ii) LSI (iii) data transmission	