Name : ....

Roll No. : ....

Invigilator's Signature : ....

CS/B.Tech (EE-N)/SEM-4/EC(EE)-402/2010

2010

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The 2's complement of the number $(01100111)_2$ is

a) 10011000 b) 10011001

c) 01100100 d) 01010111.

ii) The binary equivalent of the decimal number $(42 \cdot 6875)_{10}$ is

a) $(101010 \cdot 0100)_2$ b) $(011001 \cdot 1101)_2$

c) $(010101 \cdot 1011)_2$ d) $(101010 \cdot 1011)_2$.

iii) $(x' + y')$ can be written as

a) (xy') b) $(x+y)'$

c) $x'y'$ d) $(xy')'$

iv) The type of ROM that can be reprogrammed by ultraviolet light is called

a) PROM b) EEROM

c) EPROM d) none of these.

v) A 4-bit parallel adder can add

a) two 4-bit binary numbers

b) two 2-bit binary numbers

c) four bits at a time

d) four bits in sequence.

vi) Which flip-flop acts as a buffer ?

a) D b) T

c) J-K d) None of these.

vii) Full form of FPGA is

a) Full Programmable Gated Array

b) Field Programmable Gated Array

c) Full Peripheral Gated Array

d) Field Peripheral Gated Array.

viii) Gray code for $(1011)_2$ is

a) 1000 b) 1100

c) 1110 d) none of these.

ix) 8421 is a

a) non-weighted code

b) weighted code

c) complementary code

d) none of these.

x) In general, a multiplexer has

a) one data input, several data outputs and selection inputs

b) one data input, one data output and one selection input

c) several data inputs, several data outputs and selection inputs

d) several data inputs, one data output and selection inputs.

xi) The modulus of a counter is

a) the number of flip-flops

b) the actual number of states in its sequence

c) the number of times it recycles in a second

d) the maximum possible number of states.

xii) The carry expression of full adder circuit is

a) $X'Y + ZX'$ b) $XY + YZ + ZX$

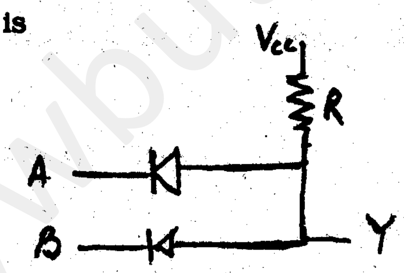
c) $XY' + YZ' + ZX$ d) $X'Y' + XZ' + YZ$.

xiii) The equation $\sqrt{213} = 13$ is valid for which one of the following number systems with base ?

a) Base 8 b) Base 6

c) Base 5 d) Base 4.

xiv) The operation of the circuit in the negative level logic system is



a) AND b) OR

c) NAND d) NOR.

xv) The flip-flop, which is free from race around problem is

a) *R-S* flip-flop

b) Master-slave *JK* flip-flop

c) *J-K* flip-flop

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw EX-OR gate circuit using minimum number of NAND gates and NOR gates.

3. Implement a 16 : 1 MUX using only 4 : 1 MUX. Show block diagram only.

4. Design and implement a full-adder circuit using a decoder and other necessary logic gates. Assume that the decoder has all active low outputs.

5. What is lock-out condition of a counter and how can we overcome it ? 3 + 2

6. What are the specifications of D/A converter ?

7. Implement the function $F(A, B, C) = \Sigma m(0, 1, 4, 6)$ using all NOR gates.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

8. a) Simplify the logic function using Quine-McCluskey method :

$F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

b) What is Don't care condition ? How is it useful to simplify a Boolean expression ? Simplify the function $F(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$.

10 + 5

9. a) Design a 3-bit synchronous counter using J-K flip-flops.

b) Design a 3-bit binary UP/DOWN counter with a direction control *M*. Use *J-K* flip-flops in your design.

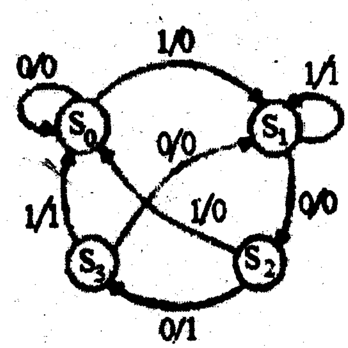
7 + 8

10. a) Describe the working principle of *R*-2*R* ladder *D*/*A* converter.

b) What is a *Sample and Hold* circuit ? Why do we need to use this circuit ? 10 + 5

11. a) What is the difference between a Mealy and Moore type sequential circuits ?

b) Design a sequential circuit that implement the following state diagram. Use all *D*-type flip-flops for the design.



c) Describe the basic principles of successive approximation method for *A*/*D* coverter. 3 + 7 + 5

12. Write short notes on any *three* of the following : 3 × 5

a) EPROM

b) Odd parity generator

c) Carry Look Ahead

d) Dual slope ADC

e) Multiplexer

f) SOP and POS canonical forms of binary function.