BE1-R3: EMBEDDED SYSTEMS

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Compare and contrast between embedded computing system and general-purpose computer.

b) What are the major levels of abstraction in the top-down design process of embedded systems?

c) Comment on the following statement – "Often the embedded system design process is also called the embedded system design cycle."

d) Compose 1k x 8 ROMs into 2k x 16 ROMs.

e) Justify the necessity of distinguishing the step system integration involved in embedded system design process.

f) Given a choice to select RISC or CISC microcontroller, which one is preferred for embedded applications and why?

g) Explain one reason using a DMA (Direct Memory Access) controller might improve a system's performance.

(7x4)

2.

a) Characterize embedded computing applications in terms of -

i) providing sophisticated functionality,

ii) costs, and

iii) performing to meet deadlines.

b) Highlight the challenges involved in embedded computing system design.

(12+6)

3.

a) Describe the need for security in Bluetooth system. How Bluetooth wireless protocol is differentiated from IrDA?

b) "Concurrent programming is said to be harder than sequential programming." – Do you agree with the statement? – Justify.

(12+6)

4.

a) Explain, why triangular routing is used in Mobile IP. What is the main problem with the route optimization?

b) We are given tasks T_1 and T_2. What does it mean to say that they execute concurrently?

c) Explain, how Port-based I/O is different from Bus-based I/O.

(10+4+4)

5.

a) Design a CMOS circuit for the full adder, where

i) A_n, B_n and C_n are three input variables,

ii) Output carry C_{n+1} is a function of A_n, B_n and C_n, and

iii) Output sum S_n is a function of A_n, B_n, C_n and C_{n+1}.

b) Realize the CMOS circuit with its structural specification as given below.

The circuit consists of four transistors in series, two consecutive pMOS transistors Q_1 and Q_2 with the source of Q_1 as V_{DD}, two consecutive nMOS transistors Q_3 and Q_4 with the source of Q_4 as ground, and the output at the common drain of Q_2 and Q_3. In addition, the gates of Q_1 and Q_4 are common to input 1, whereas the gates of Q_2 and Q_3 are complementary to each other, with the gate of Q_2 as input 2.

(10+8)

6.

a) What do you mean by integrated chip (IC)? What do you mean by IC technology? In this context briefly explain and exemplify the different design styles involved in IC design technology.

b) State whether processor technology is independent from IC technology. How are they related?

(12+6)

7. Write short notes on any **three** of the following.

i) SHARC Link ports

ii) Application-Specific Processor

iii) Liquid crystal display controller

iv) Watchdog timer

(6x3)