

(3) Assume **suitable additional data if required.**

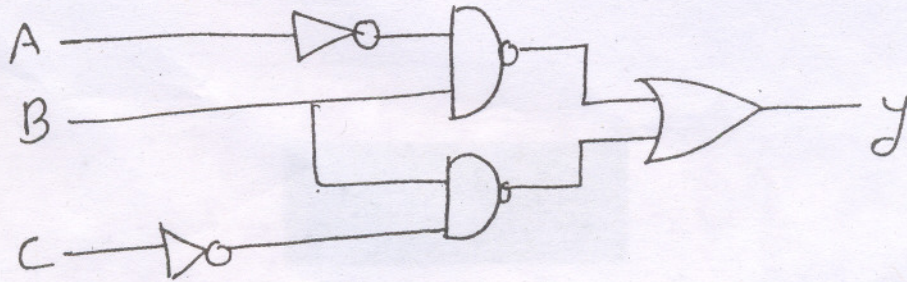
1. (a) Perform the following operations without converting to any other base. 6

(i) $(FE6)_H - (EFC)_H$

(ii) $(324)_5 \times (21)_5$

(iii) $(512)_8 + (277)_8$

(b) Determine the truth table for the circuit shown below : 4



(c) Convert SR flip-flop to D flip-flop. 5

(d) Implement following expression using only one 8:1 Multiplexer and few gates. 5

$$F = \sum m(2, 3, 5, 6, 8, 11, 13, 14, 15)$$

2. (a) Simplify the following equations using K Map. 10

(i) $A\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{D} + AB\bar{C}D + A\bar{C}\bar{D} + \bar{A}BC$

(ii) $\bar{A}\bar{D} + A\bar{B}\bar{D} + \bar{A}\bar{C}D + \bar{A}CD$

(b) Implement 32:1 multiplexer using two 16:1 multiplexer and OR gates. 10

3. (a) Minimize the following expression using Quine McCluskey tabular method : 10

$$F(A, B, C, D) = \sum m(1, 3, 5, 10, 11, 12, 13, 14, 15)$$

(b) Implement the Gray code to BCD code converter using basic gates only. 10

4. (a) Design mod 10 asynchronous up counter with the help of necessary decoding logic. 5

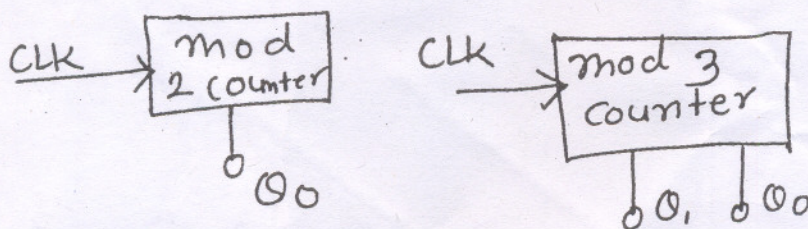
(b) Give the timing diagram for the counter of part (a). 3

(c) Explain how to convert the above counter to count down. 3

(d) If the delay of a single FF is 10 ns what will be the maximum clock frequency. 3

(e) Is glitch problem exist for above counter ? Discuss. 3

(f) Implement mod 6 counter using following two blocks. 3



5. (a) Design a 3 bit synchronous 'even' counter to give sequence of even numbers. Using D FF. Take care of lock out condition while designing. 10

(b) Design Full Subtractor circuit using active high I/p, active low O/p Decoder. 10

6. (a) Design 4 bit ring counter using JK-FF, draw the timing diagram for the same. 10

(b) Compare TTL and CMOS logic families. 10

7. (a) Design one bit BCD adder using IC 7483. 10

(b) Write short notes on (any two) :— 10

(i) Code converters

(ii) Error detecting and correcting code

(iii) ALU

(iv) Priority Encoder.