Paper ID [EC502]

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M. Tech.

ELECTRONICS SYSTEM DESIGN (EC/ECE - 502)

Time : 03 Hours   Maximum Marks : 100

Instruction to Candidates:

1)   Attempt any **Five** Questions.

2)   **All** questions carry equal marks.

Q1)   (a)   Using theorems minimize the following expression

$$F = \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}CD + \overline{A}BCD + \overline{A}B\overline{C}D + AB\overline{C}D + ABCD$$

   (b)   Simplify the following using K-map

$$F(A,B,C,D,E) = CDE + \overline{A}\,B\overline{C}\,\overline{E} + \overline{A}\,BDE + \overline{A}\,BC\overline{E}$$

Q2)   (a)   What is the need of a Comparator? Design a two bit comparator.

   (b)   Define Propagation delay? What is its significance? Also make a comparison between open collector and tri-state bus systems.

Q3)   (a)   Design a circuit to convert D Flip Flop to JK Flip Flop.

   (b)   Discuss the concept of memory. What is a binary cell? Why is it unadvisable to ASSERT both the SET and RESET input of a binary cell? Also draw a distinction between a NAND and a NOR cell.

Q4)   (a)   Why counters are used? Explain and Differentiate between single mode and multi mode operation of counters in detail.

   (b)   Why shift registers are required? Discuss the various operation modes of shift registers.

Q5)   (a)   What are the timing and frequency considerations of the controllers?

   (b)   What is understood by PAL? Explain PAL based design.

   (c)   Carry out the steps necessary to design a four way traffic light controller, one that will handle traffic flow at high rates in any of four directions. Associate a left turn with all four directions as well as a pedestrian crosswalk switch.

Q6) Explain various MEV approaches to asynchronous design in detail.

Q7) (a) Explain the various design steps of asynchronous machine.

(b) With the help of example (s) discuss the hazards in circuits developed by MEV method.

Q8) (a) Discuss how a digital system can be interfaced with fiber cables and Co-axial cables.

(b) Discuss XOR and AND-OR-Invert gates in detail.