Code No. BTS 012(C)

B.Tech. Degree V Semester Examination in Electronics and Communication Engineering, April 2000.

EC 501 MICROPROCESSORS

Time: 3 Hours *Max.Marks:100*

I a) Explain the bus structure of 8085 with a neat diagram. (10)

b) Discuss the various registers available in 8085. (10)

OR

II a) Explain the control and status signals of 8085. (12)

b) Illustrate with a neat diagram how signals $\overline{MEMR}, \overline{MEMW}, \overline{IOR}$ and $\overline{IOW}$ are generated. (8)

III a) [HL] = 213 FH, [213 FH] = 76H opcode of halt, [PC] = 2000H ; [SP] = 1800H Explain the function of the following instructions and hence write down the contents of HL, SP, PC register after their sequential execution in the following order. (10)

2000 SPHL

2001 PCHL

b) Explain the different addressing modes available in 8085 with examples for each. (10)

OR

IV a) Draw the timing diagram showing all the relevant signals for the following instruction

2000 STA 5 FFEH (12)

b) Discuss "Bus idle Machine cycles". Give examples where these cycles are used. (8)

V a) Discuss the issues in interfacing a slaw memory to the CPU. (10)

b) What is bus contention with regard to memory interfacing. Suggest method for avoiding the same. (10)

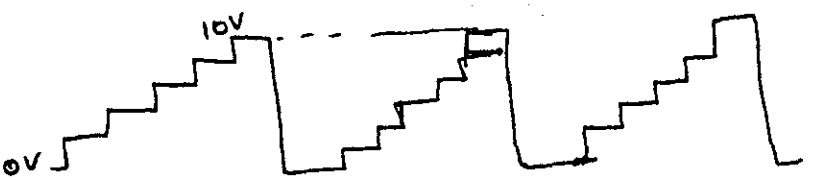
OR

VI a) Explain the different DMA modes of transfer. (10)

b) Discuss and compare the different data transfer schemes. (10)

VII a) What are vectored interrupts ? Explain with respect to 8085 CPU. (8)

b) Design a set up which will generate the following waveform. (12)



Give the necessary block diagram and program.

OR

VIII a) What are the features of Mode 1 data transfer scheme of 8255 PPI ? Explain 8255 configured as mode 1: input and give the necessary timing waveform for stribed i/p (with handshake). (14)

b) Is there a minimum pulse width required for the INTR signal ? If so what is the minimum width required for a system with 3 MHz clock frequency. (6)

IX a) Draw and explain the internal architecture of 8086 CPU. (10)

b) Explain multiprocessing ? What are its advantages ? (10)

OR

X a) Draw and explain the internal architecture of 68000 CPU. (12)

b) Differentiate between multiprocessing and multiprogramming ? (8)

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