ALCCS

AUGUST 2009
Code: CS12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Show the hardware implementation of a logic circuit that uses logic gates and generates AND, OR, XOR, complement micro-operations (one signal at a time). The selection is to be based on two input binary signals.

b. Give the steps involved in memory read operation.

c. Explain with example a two address instruction format.

d. How DRAM refresh is implemented?

e. Where is cache located in computer? What is cache hit & cache miss?

f. What is write back policy?

g. What do you understand by "Polling" in I/O subsystem design? **(7 4)**

Q.2 a. What is interrupt? Describe different types of interrupts and their use. How a processor handles a non-vectored interrupt?

b. With neat block diagram explain source initiated and destination initiated hand shaking method for data transfer. State its disadvantages, if any. **(10+8)**

Q.3 a. Explain the Restoring algorithm for division with a neat flow chart.

b. Show the register contents at each stage of multiplying with by using Booth's algorithm.
(10+8)

Q.4 a. Differentiate between
(i) Isolated and Memory mapped I/O.

(ii) Associative mapping & Direct mapping.

b. Describe the function of DMA controller in data transfer between I/O & memory. State different modes of DMA operation. **(10+8)**

Q.5 a. What do you understand by the term "Micro-operation"? Explain different types of Micro-operations with examples. Implement the following Micro-operation by using common bus & tristate buffer.

Assume M, A, Y & S to be single bit registers.

b. What is a vertical microcode? State the design strategy of vertical microcoded control unit. **(12+6)**

Q.6 a. Design a three bit combinational incrementer circuit. Also give the block circuit of the sequential incrementer.

b. Consider a cache and main memory with following specifications:-

: 16K words, 50ns access time.

: 1M words, 400 ns access time.

The size of each cache block is 8 words and the set size is 256 words with set associative mapping.

Show the mapping between & and calculate effective memory access time with cache hit ratio 0.9.

(8+10)

Q.7 Write notes on the followings:-

(i) Characteristics of RISC processor.

(ii) Address sequencing.

(iii) Synchronous & Asynchronous type data transfer. **(6 3)**