ALCCS

Code: CS12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

SEPTEMBER 2010

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. A given program consist of 50 instruction loop that is executed 42 times. It takes 8,000 cycles to execute the program on a given system. Find the computer performance in CPI (cycles per instruction)

b. Describe briefly different types of interrupts.

c. With a diagram show how subtraction can be implemented in hardware?

d. What is overflow and underflow? How these are handled by the system?

e. Using 8 bit 2's complement integers, perform the following operations:-
(i) $-34 + (-12)$ (ii) $18 - (-5)$

f. State the advantages of a stack based organisation and a general purpose register organisation.

g. What do you understand by programmed I/O? **(7 × 4)**

Q.2 a. With neat diagram show a combinational array multiplier for four bit multiplicand & four bit multiplier. Determine the output signals generated by every adder cell to compute
$(x \times y)$ for x = 1010 & y = 1001.
(10)

b. Give the flow chart for booth's multiplication and discuss how it is faster than array multiplier. **(8)**

Q.3 a. State the expected features of an Instruction set of a system. Discuss different classifications of Instruction based on format, addressing modes and types.
(10)

b. Using 2 address instruction style show how the following can be evaluated?

X = A/ (B – D) + C

(8)

Q.4 a. What is shift micro-operation? Explain logical shift, circular shift and arithmetic shift micro operation and their practical use.

(6)

b. Register A holds the 8- bit binary 11011001. Determine the B operand and the logic micro- operation to be performed in order to change the value of A to 01101101.

(4)

c. Show the organization of a micro programmed control unit and explain its operation.

(8)

Q.5 a. With a neat flow chart explain the operations involved in an interrupt cycle.

(8)

b. There are four resisters A, B, C & D. Design a common bus data path with necessary logic circuit to perform the transfer of content of any register to self or any other registers. Draw the logic circuit neatly.

(10)

Q.6 a. A computer Employs RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2k bytes of RAM, 4k bytes of ROM and four interface units, each with four registers. A memory mapped I/O configuration is used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.

(i) How many RAM & ROM chips are needed?
(ii) Draw a memory address map for the system.
(iii) Give the address range in hexadecimal for RAM, ROM and interface.

(10)

b. What is cache memory? Discuss the different mappings used in cache organization with their advantages & disadvantages.

(8)

Q.7 a. A virtual memory system has an address space of 8k words, a memory space of 4k words, and page & block size of 1k words. The following page reference changes occur during a given time interval. Determine four pages that are resident in main memory after each page reference change if the replacement algorithm used is

(i) FIFO (ii) LRU.

Page reference order:- 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7.
(10)

b. Discuss Daisy- chaining priority to handle interrupts in detail with the help of a diagram.

(8)