ALCCS

FEBRUARY 2009

Code: CS12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 **(7 x 4)**

a. What do you mean by Micro-operation, Microinstruction and Micro-program?

b. State the types of Shift operation and their use in programming.

c. What are PROM and EPROM? State the configurations and use.

d. Using 1 x 4 Demultiplexer block construct a 1 x 16 Demultiplexer.

e. Give the implementation of a three variable majority function by using suitable MUX.

f. What do you mean by Reverse Polish Notation? Represent A (B/[C+D]) using this notation.

g. How is LRU replacement technique implemented in cache memory?

Q.2 a. Discuss the principle of operation and role of Stack memory in program execution. State the microinstructions executed in stack operation.

b. Discuss the different modes of addressing used in assembly level programming. Give an example of each. **(10+8)**

Q.3 a. Discuss different sources of Interrupts. Give their application.

b. What is conditional branching? How it is executed? Give an example. **(10+8)**

Q.4 a. Draw the control unit of a basic computer. Using RTL, show how fetch and decode phases are carried out.

b. With neat block diagram, discuss the working of Microprogramme sequencer. **(8+10)**

Q.5 a. With a neat flow chart discuss the process of subtraction of floating point numbers.

b. Give the data flow through registers used in hardware realization of restoring division algorithm while dividing (10100011) by (1011). **(8+10)**

Q.6 a. With necessary block diagram, explain the DMA data transfer scheme.

b. Using two address instruction format give an assembly language program to evaluate the following expression:

(8+10)

Q.7 a. What is Virtual memory? How it is implemented in computer system?

b. A digital computer system has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block and words fields of the address format?

(ii) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.

(iii) How many blocks the cache can accommodate? **(8+10)**