Roll No.........................

Total No. of Questions : 09]

[Total No. of Pages : 02

Paper ID [B0111]

(Please fill this Paper ID in OMR Sheet)

MCA (Sem. - 3rd)

COMPUTER SYSTEM ARCHITECTURE (MCA - 301)

Time : 03 Hours

Maximum Marks : 60

Instruction to Candidates:

1) Attempt any one question from Section - **A, B, C & D**.
2) Section - E is **Compulsory**.
3) Use of Non-Programmable **Scientific Calculator** is allowed.

Section - A

(1 x 10 = 10)

Q1) (a) Explain the JK master slave flip-flop.

(b) Simplify the expression x = (A+B') (A'+B'+D')D.

(c) Solve the expression $Z(A,B,C,D) = \sum(0,1,3,5,8,9,10,13,14,15)$ using K-map.

Q2) (a) Design a MOD 11 Counter using J-K Flip Flop and NAND Logic Gates.

(b) Design the 8-Bit full adder Circuit.

Section - B

(1 x 10 = 10)

Q3) Design the Arithmetic Circuit of a processor with truth table.

Q4) (a) An 8-Bit register has one input x, the register operation is described symbolically as :

$P : A_8 \leftarrow x, A_i \leftarrow A_i+1 \quad 1 = 1,2,3, ..., 7.$

What is the function of the register? The cells are Numbered from right to Left.

(b) Using the Quadruple 2 to 1 line Multiplexer and Four Inverters, Draw a Block diagram for implementing the statement.

$T_1 : R_2 \leftarrow R_1$

$T_2 : R_2 \leftarrow R_2$

$T_3 : R_2 \leftarrow 0.$

Section - C

(1 x 10 = 10)

Q5) (a) Write a micro program that compares two unsigned binary number stored in R_1 & R_2. The register containing the greater number is then cleared. If the two numbers are equal, both numbers are cleared.

(b) Explain the following :

i) microoperation.

ii) micro instructions.

iii) microprogram.

Q6) A computer has 16 registers an ALU with 32 operations and a Shifter with eight operations all connected to common Bus system.

(a) Formulate a control word for a microoperation.

(b) Specify the number of bits in each field of control word and give an encoding scheme.

(c) Show the bits of the control word that specify the microoperation $R_4 \leftarrow R_5 + R_6$.

Section - D

(1 x 10 = 10)

Q7) (a) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes.

(b) How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips.

(c) How many lines must be decoded for chip select? Specify the size of decoders.

Q8) (a) Explain the Cache memory.

(b) Explain Associative memory.

Section - E

Q9) a) Draw the logic circuit for y = (a'+b'+c) (a'+b+c') using any of the universal Gate. **(2)**

b) Suppose a ROM has 16 input address lines. How many memory location does it have, Range them. **(2)**

c) Convert the 1234 BCD its Octal equivalent. **(2)**

d) Name the various Addressing Modes for pointing a data in a memory location. **(3)**

e) Explain the constituents of an Instruction Cycle. **(3)**

f) What is a Virtual memory? **(4)**

g) Differentiate between Microprogramming and Hardwired control unit. **(4)**

✷ ✷ ✷