SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E – EEE
Title of the paper: Computer Aided Design
Semester: V — Max.Marks: 80
Sub.Code: 414507 — Time: 3 Hours
Date: 04-05-2009 — Session: AN

PART – A (10 x 2 = 20)

Answer All the Questions

1. What is the acronym for MATLAB and VHDL?

2. Write the syntax of format function with an example.

3. Mention the advantages of M-File scripting.

4. Debug the following code:

```
t= -pi:pi/100:pi;
y= sin(t);
plot(t,y,-r);
axis ([-pi pi -1 1]);
xlabel (‘”\pi \leg {\itt} \leg \pi”);
ylabel (‘sin(t)’;
```

5. Write an M-file to simulate and plot an ideal half wave rectifier with v(x) = 12 sin (x).

6. What is meant by closed-loop simulation? Mention their advantages.

7. What are the standard IEEE libraries used in VHDL coding?

8. What are physical types of data? Give an example.

9. Why we go for VHDL for real time design and simulation of digital system?

10. What is a Test bench in VHDL?

PART – B (5 x 12 = 60)

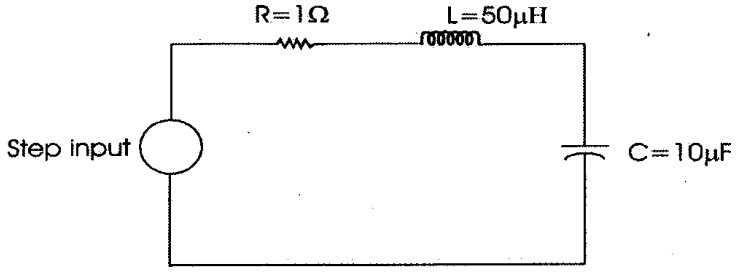
Answer All the Questions

11. Write M-files to
    (a) Generation 5x5 random matrix.
    (b) Solve the quadratic equation.
    (c) Scalar multiplication of matrices.
    (d) Generate first 10 Fibonacci numbers. (4x3=12)

(or)

12. (a) Explain in detail about the colon (:) operator with an example.
    (b) Draw the mesh plot for sinc function using plotting command in MATLAB?

13. For the given RLC series network,



Develop the MATLAB-Simulink model for obtaining the time response characteristics of the system.

(or)

14. Write M-File for simulation of n-point DFT using Cooley-Tukey algorithm (FFT) with two radix butterfly as its basic function.

15. Assume that a BJT has an emitter area of 5.0mil^2, β_F = 120, β_R = 0.3, transport current density, J_S = 2 x 10^{-10} μA/mil^2 and T =

300K. Plot I_E versus V_{BE} for V_{BC} = -1V using MATLAB. Assume $0 < V_{BE} < 0.7$ V, $q=1.602 \times 10^{-19}$.

(or)

16. For the circuit shown in Fig.1, use MATLAB to find the poles and zeros. Plot the magnitude and phase response, assume that C1 = 0.1uF, C2 = 1000 0.1uF, R1 = 10K, and R2 = 10Ω.

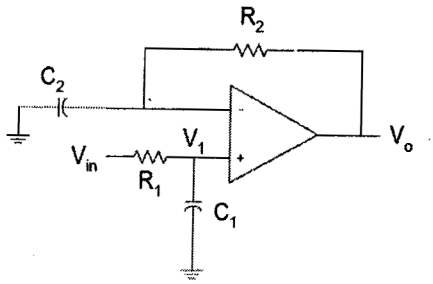


Fig.1

$$\frac{V_o}{V_{IN}}(s) = \frac{C_2R_2\left(s+\frac{1}{C_2R_2}\right)}{C_1R_1\left(s+\frac{1}{C_1R_1}\right)}$$

Transfer function

17. (a) Describe about mixed style modeling and implement Full adder with mixed style model of VHDL.
(b) Briefly explain about assertion statement with raising edge triggered D flip-flop as its example.

(or)

18. Design a 4-bit ALU unit of a microprocessor with
(a) Carry and borrow overflows
(b) Signed and unsigned overflows
(c) All basic arithmetic and logical operations
(d) Increment and decrement operations using VHDL coding

19. (a) Explain briefly about operator overloading with an example.
(b) Write down the steps to create the user defined libraries.

(or)

20. (a) Write VHDL code to find largest of two 8-bit binary number. (5)
(b) What are the Effects of Transport delays on signal drivers? (3)
(c) Write steps to create a state machine using VHDL. (4)