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## AMIETE -CS/IT (OLD SCHEME)

Time: 3 Hours

## DECEMBER 2011

Max. Marks: 100
Time. 3 Hours

NOTE: There are 9 Questions in all.

- Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.
- Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the $\mathbf{Q} .1$ will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.
Q. 1 Choose the correct or the best alternative in the following:
a. Which of the following is trivalent?
(A) Arsenic
(B) Aluminum
(C) Phosphorus
(D) Bismuth
b. The value of load resistor in this circuit (Fig.1) is if current through the diode is 2 mA
(A) 5 K
(B) 5.5 K
(C) $5.5 \Omega$
(D) 4.5 K

c. Identify the output of the following circuit shown in Fig. 2
(A) AND
(B) XOR
(C) XNOR
(D) NOR


Fig. 2
d. When simplified the result of expression $y=(\bar{A}+B)(A+B)$ is $\qquad$
(A) $\bar{B}$
(B) B
(C) A
(D) AB
e. A Zener diode has dc power dissipation rating of 50 mW and Zener voltage rating of 7.5 V The value of $\mathrm{I}_{\mathrm{ZM}}$ is
(A) 76.76 mA
(B) 66.67 mA
(C) 76.68 mA
(D) 67.86 mA
$\qquad$
f. In ECL logic family the logic swing with 5 V power supply is $\qquad$
(A) less than 2 V
(B) 3.6 V
(C) 5 V
(D) 4 V
g. For a transistor $\beta=40, I_{B}=25 \mu \mathrm{~A}$, the value of $\mathrm{I}_{\mathrm{E}}$ will be
(A) 1 mA
(B) 1.025 mA
(C) 0.975 mA
(D) $1.25 \mu \mathrm{~A}$
h. The opamp circuit shown in Fig. 3 is
(A) Inverting Amplifier
(B) Voltage Follower
(C) Summer
(D) Active half wave


Fig. 3
i. How many 16 K X 4 RAMS are required to achieve a memory with a capacity of 64 K and word length of 8 bits?
(A) 4
(B) 8
(C) 6
(D) 16
j. MOS circuits as compared to bipolar circuits take $\qquad$
(A) same chip area
(B) less chip area
(C) more chip area
(D) none

## Answer any FIVE Questions out of EIGHT Questions. <br> Each question carries 16 marks.

Q. 2 a. Draw a neat schematic representation of p-n junction and explain what happens when junction is (i) forward biased (ii) reverse biased. Draw the practical VIcharacteristics of pn-junction diode and discuss the effect of temperature on current flowing through the diode?
b. With neat circuit diagram and input-output waveforms explain FET works as a switch?
c. (i) Find the values of $\mathrm{V}_{\mathrm{L}}, \mathrm{V}_{\mathrm{R}}, \mathrm{I}_{\mathrm{Z}}$ and $\mathrm{P}_{\mathrm{Z}}$ in the Zener network shown below in Fig. 4


Fig. 4
$\qquad$
(ii) Sketch correct output waveform for the following circuit:


Fig. 5
Q. 3 a. Compute the overall voltage gain for the two stage-RC coupled amplifier shown in the Fig.6. Assume $\mathrm{V}_{\mathrm{BE}}=0.7 \mathrm{~V}$ and $\beta_{1}$ (of Q1) $=\beta_{2}$ (of Q2) $=100$ (Hint:-Use $r_{e}$ model)

b. Draw a neat circuit and prove that current gain in Darlington amplifier is $\beta^{2} \mathbf{( 4 )}$
c. Given the following hybrid- $\pi$ parameters for the transistor at $\mathrm{I}_{\mathrm{C}}=10 \mathrm{~mA}$, $\mathrm{V}_{\mathrm{t}}=0.026 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=10 \mathrm{~V}$ and room temperature $\mathrm{h}_{\mathrm{fe}}=100, \mathrm{~h}_{\mathrm{ie}}=500 \Omega, \mid \mathrm{Ail}=10$ at $10 \mathrm{MHz}, \mathrm{C}_{\mathrm{C}}=3 \mathrm{pF}$. Find the values of (i) $\mathrm{r}_{\mathrm{b}^{\prime} \mathrm{e}}$ (ii) $\mathrm{r}_{\mathrm{bb}}$ (iii) $\mathrm{f}_{\mathrm{T}}$ and (iv) $\mathrm{f}_{\beta}$ (4)
Q. 4 a. Determine $I_{D}$ and $V_{D S}$ if $V_{P}=-4 V$ and $I_{D S S}=10 \mathrm{~mA}$ for the following circuit shown in Fig.7:


Fig. 7

## ROLL NO.

## Code: AC03 / AT03 Subject: BASIC ELECTRONICS \& DIGITAL CIRCUITS

b. A voltage $200 \cos 100 t$ is applied to a half wave rectifier circuit having load resistance of $5 \mathrm{~K} \Omega$.Rectifier may be represented as an ideal diode in series with resistance of $1 \mathrm{~K} \Omega$. Find (i) Average value of current through the load and voltage across the load (ii) RMS current (iii) Rectifier efficiency (iv) PIV
c. Design LC filter for full wave rectifier to provide output of 25 V with load current of 100 mA and its ripple limited to $3 \%$.
Q. 5 a. With neat circuit and input/output waveforms indicate how operational amplifier works as inverting and non-inverting amplifier derive expression for gain in each case.
b. Draw the circuit of Wien bridge oscillator and derive the expression for frequency of oscillations. List advantages and disadvantages of this circuit.(8)
Q. 6 a. Prove using Boolean laws that If $\bar{A} B+C \bar{D}=0$ then expression $A B+\bar{C}(\bar{A}+\bar{D})=A B+B D+\bar{B} \bar{D}+\bar{A} \bar{C} D$
b. Simplify using K-map and realize the result using only NOR gates. $f(A, B, C, D)=\prod(0,1,2,3,7,8,9,10,11)+d(6,14,15)$
c. Design $4: 1$ multiplexer using NAND gates only
Q. 7 a. Explain basic TTL circuit and compare it with DTL in brief
b. List any four characteristics ECL logic family.
c. Sketch the circuit and characteristics of CMOS inverter and verify truth table for NOT operation.
Q. 8 a. Sketch the circuit for SR flip-flops using NAND gates. Draw the truth table and obtain characteristic equation for the SR flip-flop .How to convert it into T flip-flop?
(8)
b. Show how a modulo-4 counter designed with two flip-flops can generate a repetitive sequence of binary word 1101 with minimum number of memory elements?
Q. 9 a. Discuss any six applications of ROM.
b. What is latency time in CCD memory? Explain CCD memory organization in brief.
c. What is Random Access Memory? How are they classified? List its advantage \&.disadvantage with respect to ROM.
d. How PLAs are different from ROM? Explain

