Karunya University

(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – November/December 2011

Subject Title: **SOLID STATE CIRCUITS - II**   Time: 3 hours
Subject Code: **EC206**   Maximum Marks: 100

Answer ALL questions
PART – A (10 x 1 = 10 MARKS)

1. Define rise time.
2. What is meant by amplitude slicer?
3. What are the triggering methods?
4. What is the effect of loading?
5. Define transition time.
6. What is VCO?
7. Define Displacement error.
8. Where are the time base generators used?
9. What is blocking oscillator?
10. What is an ideal sampling gate?

PART – B (5 x 3 = 15 MARKS)

11. What is synchronized clamping?
12. What is commutating capacitors?
13. Write the timing equation for mono stable and astable circuits.
14. List the methods of generating a time base generators.
15. What are the applications of blocking oscillators?

PART – C (5 x 15 = 75 MARKS)

16. Draw the response of high pass circuit for square wave input and derive the expression for percentage tilt.

(OR)

17. How do the high pass circuit act as a differentiator and low pass circuit act as an integrator?

18. Explain the operation of self-biased transistor bistable multivibrator with neat circuit diagram.

(OR)

19. What is Schmitt trigger circuit? Explain its operation with neat circuit diagram and applications.

20. Explain the operation of a collector coupled mono stable multivibrator and also derive the expression for gate width.

(OR)

21. Explain the operation of an emitter coupled astable multivibrator with its waveforms.

22. Explain how a constant current sweep is generated using transistor and determine the expression for slope error.

(OR)

23. Explain the transistor television sweep circuit with waveforms.

24. Explain a triggered transistor-blocking oscillator with base timing and also derive the expression for pulse width.

(OR)

25. Explain with examples unidirectional and bidirectional sampling gates.