Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M.E -III[rd] SEMESTER–EXAMINATION – MAY- 2012

Subject code: 730303 Date: 10/05/2012

Subject Name: VLSI Design

Time: 10:30 am – 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Consider Moore Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "101" input bit sequence. Implement the state diagram for above and write verilog code for it.	**14**
Q.2	**(a)**	What are the different rules that are to be used while developing UDPs?	**07**
	(b)	Explain features of XC9500 Programmable CPLD family in brief.	**07**
		OR	
	(b)	Explain mux- versus LUT-based logic blocks.	**07**
Q.3	**(a)**	Explain various behavioral timing control constraints available in verilog	**07**
	(b)	Explain ROM, PAL, PLA and PLD by comparing with eachother.	**07**
		OR	
Q.3		Explain the architecture of Spartan3e FPGA family	**14**
Q.4	**(a)**	Write a verilog program for 8 input priority encoder.	**07**
	(b)	When race condition occurs in verilog? Explain with example.	**07**
		OR	
Q.4	**(a)**	Write a verilog program for full-subtractor using half-subtractor and logic gates. Write modules for half-subtractor and the gates used. Draw the circuit diagram of the whole design.	**07**
	(b)	Explain the use of casex, casez in verilog with example.	**07**
Q.5		With the help of T-flipflop design a modulo 6 counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design. Dtaw the circuit diagram of your design.	**14**
		OR	
Q.5		With the help of T-flipflop design a binary counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design.	**14**

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