Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –III Examination Dec. - 2011

Subject code: 730303 **Date: 08/12/2011**

Subject Name: VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Design 4-bit full-adder with the help of 4 1-bit full-adders using structural model. Write verilog program for the same. Write module for 1-bit full adder also. Draw block diagram of your design.	**14**
Q.2	**(a)**	Explain features of Spartan3e FPGA family in brief.	**07**
	(b)	State the difference between antifuse and SRAM based FPGAs.	**07**
		OR	
	(b)	What is race condition in verilog? How it can be eliminated?	**07**
Q.3	**(a)**	Explain delay-based timing control in verilog along with appropriate example.	**07**
	(b)	State rules for developing UDPs.	**07**
		OR	
Q.3		Explain in detail the architecture of XC9500 Complex Programmable Logic Devices.	**14**
Q.4		Design counter having output sequence of 0,2,7,1,3,0…. so on repeating using T flipflop with the help of flipflop excitation table. Show all design steps. Write verilog program of the same using structural model style. Write modules for all the components used in your design. Draw the ckt diagram for the design.	**14**
		OR	
Q.4		Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "111" input bit sequence. Implement the state diagram for above and write verilog code for it.	**14**
Q.5	**(a)**	Write verilog program for 4-bit up-down counter with load facility. Draw the circuit diagram for the same.	**07**
	(b)	Compare the following: (1) Tasks and Functions (2) CPLD and FPGA	**07**
		OR	
Q.5	**(a)**	Write a verilog program for 8x1 mux using case statement.	**07**
	(b)	Explain in detail different operator types in verilog.	**07**

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