Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. Sem. – III - Examination –June- 2011

Subject code: 730303

Subject Name: VLSI Design

Date:07/06/2011 **Time: 10.30 am – 01.00 pm**

Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain FPGA Spartan 3e family architecture with its components and neat diagram.	**07**
	(b)	Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "110" input bit sequence. Implement the state diagram for above and write verilog code for it.	**07**
Q.2	**(a)**	Explain functions of digital clock managers in regards to Spartan 3e.	**07**
	(b)	Compare ROM, PAL, PLA and PLD.	**07**
		OR	
	(b)	With diagram explain FUSE and ANTIFUSE mechanism of FPGA programming.	**07**
Q.3	**(a)**	Explain in detail different operator types in verilog.	**07**
	(b)	Write a verilog program for full subtractor in structural modeling.	**07**
		OR	
Q.3	**(a)**	Explain the difference between net and register in verilog with appropriate example.	**07**
	(b)	Write a verilog program of 3-to-8 decoder with enable input.	**07**
Q.4		With the help of T-flipflop design a decade counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design.	**14**
		OR	
Q.4		With the help of T-flipflop design a modulo 7 counter. Show all design steps. Write verilog program of the same using structural model style. Also write verilog program of all components used in your design.	**14**
Q.5	**(a)**	Explain in detail different timing controls in verilog.	**07**
	(b)	Write a verilog program for 4-to-1 multiplexer using case statement.	**07**
		OR	
Q.5	**(a)**	What do you mean by race condition in verilog. Explain with appropriate example.	**07**
	(b)	Define a positive-edge triggered D-flipflop with clear as a UDP. Signal clear is active low	**07**

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