Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**M.E Sem-III Regular Examination January 2011**

**Subject code: 730303 Subject Name: VLSI Design**

**Date: 10 /01 /2011 Time: 02.30 pm – 05.00 pm**

**Total Marks: 70**

## Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

**Q.1** **(a)** With the help of neat diagram explain architecture of XC9500 CPLD in detail. **07**

**(b)** Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "0101" input bit sequence. Overlapping sequences are accepted, i.e." if input X is 01010100.....output Z is 00010100." Implement the state diagram for above and write verilog code for it. **07**

**Q.2** **(a)** Compare the following: **07**

I Moore and Mealy machines. II CPLD and FPGA

**(b)** Explain in detail different configuration modes of FPGA. **07**

**OR**

**(b)** What do you mean by block RAM and distributed RAM? Explain internal structure of block RAM of sparten3e FPGA. **07**

**Q.3** **(a)** With the help of T-flipflop design a counter that gives 0, 1, 4, 6, 7, 0, 1….. so on as an output sequence. Show all design steps. Write verilog program of the same using structural model style. **07**

**(b)** Write a verilog program of 2x4 decoder with enable input. When enable input is inactive then output should be in high impedance. **07**

**OR**

**Q.3** **(a)** Draw the ckt of 32x1 multiplexer using 8x1 multiplexer, 2-to-4 decoder and basic gates. Write verilog program for the same. **07**

**(b)** Write a verilog program of full adder using half-adders and logic gates **07**

**Q.4** **(a)** Write a verilog program for 8-bit Universal shift register with shift right, shift left and parallel load capabilities. **07**

**(b)** Explain the use of casex, casez in verilog with example. **07**

**OR**

**Q.4** **(a)** Write a verilog program for 8 input priority encoder. **07**

**(b)** Explain in detail delay-based, event-based and level sensitive timing controls in verilog with example. **07**

**Q.5** **(a)** Answer the following: **07**

1. State the difference between antifuse and SRAM based FPGAs.
2. Write the difference between register and nets.

**(b)** Write a verilog program for 4-bit ripple counter using T flip-flop. Make use of UDP. **07**

**OR**

**Q.5** **(a)** Answer the following: **07**

1. Write any two differences between PAL and PLA?
   What size of shift register will be supported by 5-bit LUT?
2. Write the difference between tasks and functions.

**(b)** Explain blocking and non-blocking assignments in verilog with examples. **07**

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