GATE 1996

ELECTRONICS & COMMUNICATIONS ENGINEERING

Duration: 3 Hours Maximum Marks:150

Read the following instructions carefully:

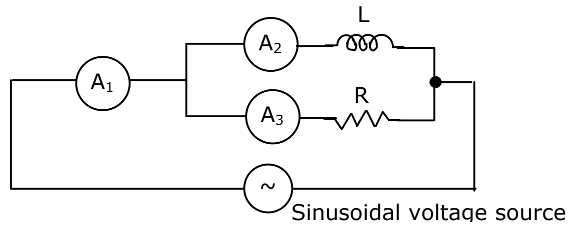
1. Write all the answers in the answer book.
2. This question paper consists of **TWO SECTIONS: A and B.**
3. **Section A** has **Eight** questions. Answer **ALL** questions in this section.
4. **Section B** has Twenty questions. Answer any **TEN** questions from this section. If more number of questions are attempted, strike off the answers not to be evaluated; else only the **FIRST TEN** unscored answers will be considered.
5. Answers to **Section B** should start on a fresh page and should not be mixed with answers to **Section A**.
6. Answers to questions and answers to parts of a question should appear together and should not be separated.
7. In all questions of 5 marks, write clearly the important steps in your answer. These steps carry partial credit.
8. There will be no negative marking.

SECTION - A

1. For each of the following questions (1.1 – 1.20), four alternatives (A,B, C and D) are given. Indicate the correct answer by writing the letter (A,B,C or D) against the corresponding question number.

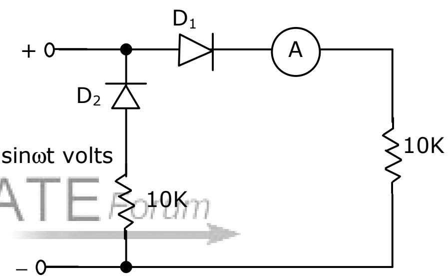
1.1 In Fig.1.1, A_1, A_2 and A_3 are ideal ammeters? If A_2 and A_3 read 3A and 4A respectively, then A_1 should read

(a) 1A
(b) 5A
(c) 7A
(d) None of the above



1.2 In the circuit of Fig.1.2, assume that the diodes are ideal and the meter is an average indicating ammeter. The ammeter will read

(a) $0.4\sqrt{2}A$
(b) 0.4A
(c) $\frac{0.8}{\pi}A$
(d) $\frac{0.4}{\pi}$



1.3 The number of independent loops for a network with a n nodes and b branches is

(a) n -1
(b) b - n
(c) b – n + 1
(d) independent of the number of nodes

1.4 A lossless transmission line having 50Ω characteristic impedance and length $\frac{\lambda}{4}$ is short circuited at one end and connected to an ideal voltage source of 1V at the other end. The current drawn from the voltage source is

(a) 0
(b) 0.02 A
(c) ∞
(d) None of the above

1.5 The p-type substrate in a conventional pn-junction isolated integrated circuit should be connected to

(a) nowhere, i.e. left floating
(b) a dc ground potential
(c) the most positive potential available in the circuit
(d) the most negative potential available in the circuit

1.6 If a transistor is operating with both of its junctions forward biased, but with the collector base forward bias greater than the emitter – base forward bias, then it is operating in the

(a) forward active mode (b) reverse saturation mode
(c) reverse active mode (d) forward saturation mode

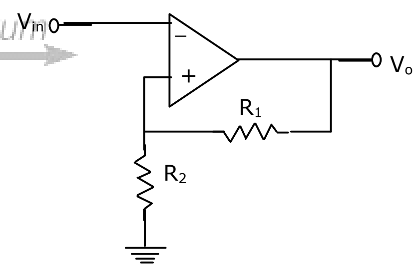
1.7 The common-emitter short-circuit current gain β of a transistor

(a) is a monotonically increasing function of the collector current I_C
(b) is a monotonically decreasing function of I_C
(c) increases with I_C, for low I_C, reaches maximum and then decreases with further increase in I_C
(d) is not a function of I_C

1.8 A n-channel silicon $\left(E_g = 1.1eV\right)$ MOSFET was fabricated using n^+ poly-silicon gate and the threshold voltage was found to be 1V. Now, if the gate is changed to p^+ poly-silicon, other things remaining the same, the new threshold voltage should be

(a) -0.1 V (b) 0 V (c) 1.0 V (d) 2.1 V

1.9 The circuit shown in Fig.1.9 is that of



(a) a non-inverting amplifier
(b) an inverting amplifier
(c) an oscillator
(d) a Schmitt trigger

1.10 Schottky clamping is resorted in TTL gates

(a) to reduce propagation delay (b) to increase noise margins
(c) to increase packing density (d) to increase fan-out

1.11 A pulse train can be delayed by a finite number of clock periods using

(a) a serial-in serial-out shift register
(b) a serial-in parallel-out shift register
(c) a parallel-in serial-out shift register
(d) a parallel-in parallel-out shift register

1.12 A 12-bit ADC is operating with a 1μsec clock period and the total conversion time is seen to be 14μsecs. The ADC must be of the

(a) flash type (b) counting type
(c) integrating type
(d) successive approximation type

1.13 The total number of memory accesses involved (inclusive of the op-code fetch) when an 8085 processor executes the instruction LDA 2003 is

(a) 1 (b) 2 (c) 3 (d) 4

1.14 The trigonometric Fourier series of an even function of time does not have the

(a) dc term
(b) cosine terms
(c) sine terms
(d) odd harmonic terms

1.15 The Fourier transform of a real valued time signal has

(a) odd symmetry
(b) even symmetry
(c) conjugate symmetry
(d) no symmetry

1.16 A rectangular pulse of duration T is applied to a filter matched to this input. The output of the filter is a

(a) rectangular pulse of duration T
(b) rectangular pulse of duration 2T
(c) triangular pulse
(d) sine function

1.17 The image channel rejection in a superheterodyne receiver comes from

(a) IF stages only
(b) RF stages only
(c) detector and RF stages only
(d) detector RF, and IF stages

1.18 The capacitance per unit length and the characteristic impedance of a lossless transmission line are C and Z_o respectively. The velocity of a traveling wave on the transmission line is

(a) Z_oC (b) $\frac{1}{Z_oC}$ (c) $\frac{Z_o}{C}$ (d) $\frac{C}{Z_o}$

1.19. A transverse electromagnetic wave with circular polarization is received by a dipole antenna. Due to polarization mismatch, the power transfer efficiency from the wave to the antenna is reduced to about

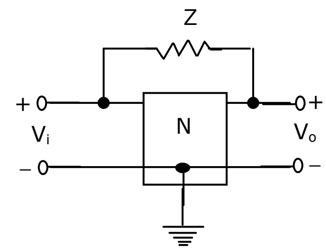
(a) 50% (b) 35.3% (c) 25% (d) 0%

1.20. A metal sphere with 1m radius and a surface charge density of 10 Coulombs/m^2 is enclosed in a cube of 10m side. The total outward electric displacement normal to the surface of the cube is

(a) 40π Coulombs
(b) 10π Coulombs
(c) 5π Coulombs
(d) None of the above

2. For each of the following questions (2.1 – 2.20), four alternatives (A, B, C and D) are given. Indicate the correct answer by writing the letter (A, B, C or D) against the corresponding question number.

2.1 In the circuit shown in Fig.2.1, N is a finite gain amplifier with a gain of k, a very large input impedance, and a very low output impedance. The input impedance of the feedback amplifier with the feedback impedance Z connected as shown will be



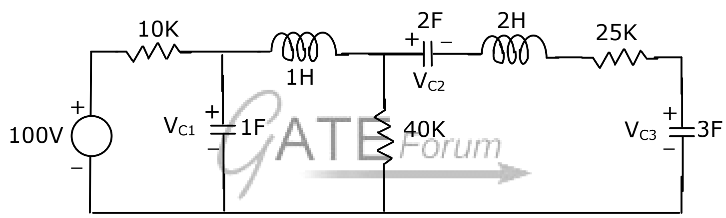
(a) $Z\left(1-\frac{1}{k}\right)$ (b) Z(1 − k)

(c) $\frac{Z}{(k-1)}$ (d) $\frac{Z}{(1-k)}$

2.2. The inverse Laplace transform of the function $\frac{s+5}{(s+1)(s+3)}$ is

(a) $2e^{-t}-e^{-3t}$ (b) $2e^{-t}+e^{-3t}$ (c) $e^{-t}-2e^{-3t}$ (d) $e^{-t}+e^{-3t}$

2.3. The voltages V_{C1}, V_{C2}, and V_{C3} across the capacitors in the circuit in Fig.2.3, under steady state, are respectively



(a) 80V, 32V, 48V (b) 80V, 48V, 32V
(c) 20V, 8V, 12V (d) 20V, 12V, 8V

2.4. A uniform plane wave in air is normally incident on infinitely thick slab. If the refractive index of the glass slab is 1.5, then the percentage of incident power that is reflected from the air-glass interface is

(a) 0% (b) 4% (c) 20% (d) 100%

2.5. In a bipolar transistor at room temperature, if the emitter current is doubled the voltage across its base-emitter junction

(a) doubles (b) halves
(c) increases by about 20 mV (d) decreases by about 20 mV

2.6. As npn transistor has a beta cutoff frequency f_β of 1 MHz, and common emitter short circuit low-frequency current gain β_o of 200. It unity gain frequency f_T and the alpha cutoff frequency f_α respectively are

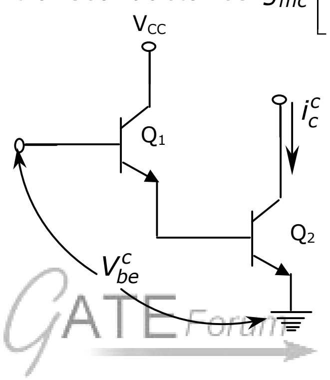
(a) 200 MHz, 201 MHz (b) 200 MHz, 199 MHz
(c) 199 MHz, 200 MHz (d) 201 MHz, 200 MHz

2.7. A silicon n MOSFET has a threshold voltage of 1V and oxide thickness of A^o. $\left[\varepsilon_r\left(\text{si}O_2\right) = 3.9, \varepsilon_o = 8.854\times10^{-14} F/cm, q = 1.6\times10^{-19} C\right]$. The region under the gate is ion implanted for threshold voltage tailoring. The does and type of the implant (assumed to be a sheet charge at the interface) required to shift the threshold voltage to −1V are

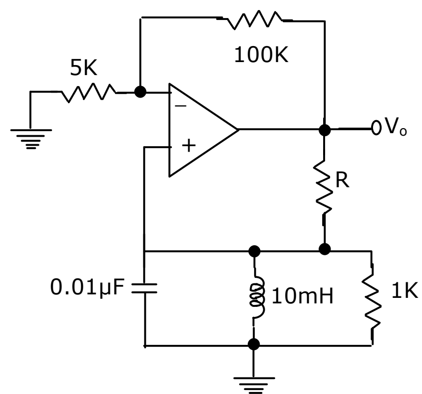
(a) $1.08\times10^{12}\ /cm^2, p-type$
(b) $1.08\times10^{12}\ /cm^2, n-type$
(c) $5.4\times10^{11}\ /cm^2, p-type$
(d) $5.4\times10^{11}\ /cm^2, n-type$

2.8. A Darlington stage is shown in Fig.2.8. If the transconductance of Q_1 is g_{m1} and Q_2 is g_{m2}, then the overall transconductance $g_{mc}\left[\Delta \frac{i_c^c}{v_{be}^c}\right]$ is given by

(a) g_{m1}
(b) $0.5\,g_{m1}$
(c) g_{m2}
(d) $0.5\,g_{m2}$,



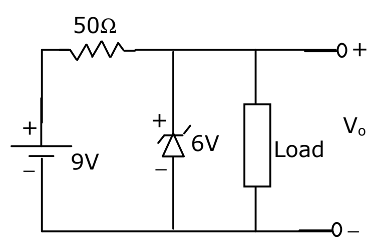
2.9. Value of R in the oscillator circuit shown in Fig.2.9, is so chosen that it just oscillates at an angular frequency of ω. The value of ω and the required value of R will respectively be



(a) 10^5 rad/sec, $2\times10^4\Omega$
(b) 2×10^4 rad/sec, $2\times10^4\Omega$
(c) 2×10^4rad/sec, $10^5\Omega$
(d) 10^5 rad/sec, $10^5\Omega$

2.10. A Zener diode in the circuit shown in Fig.2.10, has a knee current of 5 mA, and a maximum allowed power dissipation of 300mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_o constant at 6V?

(a) 0 mA, 180 mA
(b) 5 mA, 110 mA
(c) 10 mA, 55 mA
(d) 60 mA, 180 mA



2.11. A dynamic RAM cell which hold 5V has to be refreshed every 20 m secs, so that the stored voltage does not fall by more than 0.5V. If the cell has a constant discharge current of 0.1 pA, the storage capacitance of the cell is

(a) $4\times10^{-6}F$ (b) $4\times10^{-9}F$ (c) $4\times10^{-12}F$ (d) $4\times10^{-15}F$

2.12. A 10-bit ADC with full scale output voltage of 10.24 V is designed to have a ± LSB/2 accuracy. If the ADC is calibrated at 25°C and the operating temperature ranges from 0°C to 50°C, then the maximum net temperature coefficient of the ADC should not exceed

(a) ±200μV/°C (b) ±400μV/°C
(c) ±600μV/°C (d) ±800μV/°C

2.13. A memory system of size 26K bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is

(a) 2 (b) 4 (c) 8 (d) 16

2.14. The following sequence of instructions are executed by an 8085 microprocessor:

1000	LXI SP,	27 FF
1000	CALL	1006
1006	POP H	

The contents of the stack pointer (SP) and the HL, register pair on completion of execution of these instructions are

(a) SP = 27 FF, HL = 1003 (b) SP = 27 FD, HL = 1003
(c) SP = 27 FF, HL = 1006 (d) SP = 27 FD, HL = 1006

2.15. The number of bits in a binary PCM system is increased from n to n + 1. As a result, the signal to quantization noise ratio will improve by a factor

(a) $\frac{n+1}{n}$ (b) $2^{\frac{(n+1)}{n}}$
(c) $2^{\frac{2(n+1)}{n}}$ (d) which is independent of n

2.16. The autocorrelation function of an energy signal has

(a) no symmetry (b) conjugate symmetry
(c) odd symmetry (d) even symmetry

2.17. An FM signal with a modulation index 9 is applied to a frequency trippler. The modulation index in the output signal will be

(a) 0 (b) 3 (c) 9 (d) 27

2.18. The critical frequency of an ionospheric layer is 10 MHz. What is the maximum launching angle from the horizon for which 20 MHz wave will be reflected by the layer?

(a) 0° (b) 30° (c) 45° (d) 90°

2.19. A 1 km long microwave link uses two antennas each having 30 dB gain. If the power transmitted by one antenna is 1 W at 3 GHz, the power received by the other antenna is approximately

(a) 98.6μW (b) 76.8μW (c) 63.4μW (d) 55.2μW

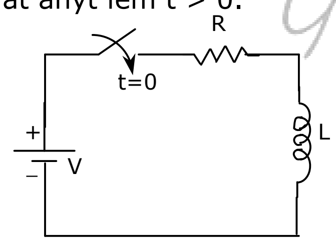
2.20. Some unknown material has a conductivity of 10^6 mho/m and a permeability of $4\pi \times 10^{-7} H/m$. The skin depth for the material at 1 GHz is

(a) 15.9 μm (b) 20.9 μm (c) 25.9 μm (d) 30.9 μm

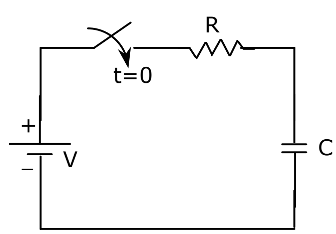
3. In the following questions (3.1 – 3.5), match each of the items 1,2 on the left with the most appropriate item a,b,c or d on the right.

3.1 In the circuit shown in Fig.3.1(a) – (c), assuming initial voltage and capacitors and currents through the indicators to be zero at the time of switching (t = 0), then at anyt iem t > 0.

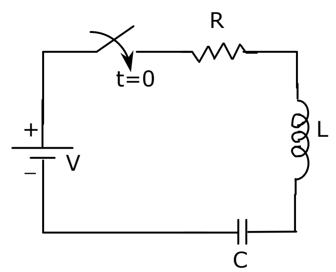
(a)



(b)



(c)



(1) Current increases monotonically with time

(2) Current decreases monotonically with time

(3) Current remains constant at V/R

(4) Current first increases then decreases

(5) No current can ever flow

3.2 (a) Cascade amplifier
(b) Differential amplifier
(c) Darlington pair common-emitter amplifier

(1) does not provide current gain
(2) is a wideband amplifier
(3) has very low input impedance and very high current gain
(4) has very high input impedance and very high current gain
(5) provides high common mode voltage rejection.

3.3 (a) A shift register can be used
(b) A multiplexer can be used
(c) A decoder can be sued

(1) for code conversion
(2) to generate memory chip select
(3) for parallel-to-serial conversion
(4) as a many-to-one switch
(5) for analog-to-digital conversion

3.4 (a) Capture effect is a characteristics of
(b) Granular noise occurs in
(c) Guard band is required in

(1) An AM system
(2) An FM system
(3) A DM system
(4) a FDM system
(5) A PCM system
(6) A TDM system

3.5 (a) SSB Modulation
(b) $\nabla \cdot \bar{B} = 0$
(c) Model dispersion

(1) Transmission line
(2) Hilbert transform
(3) Faraday's law
(4) Absence of magnetic monopoles
(5) Wave guides
(6) Phase-locked loop

4. A signal $3\sin(\pi f_o t) + 5\cos(3\pi f_o t)$ is applied to an RC low pass filter of 3 dB cut off frequency f_o. Determine and plot the output power spectrum also calculate total input and output normalized power.

5. A common emitter amplifier with an external capacitors C_C connected across the base and the collector of the transistor is shown in Fig.5.

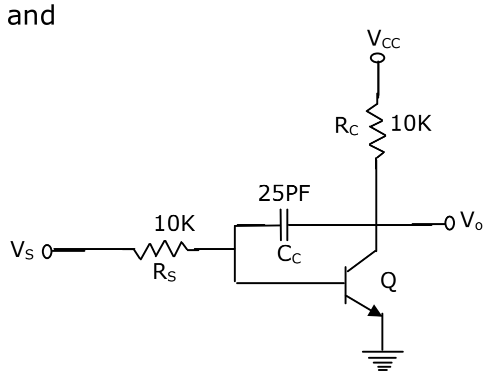
Transistor data:

$g_m = 5mA/V$

$r_\pi = 20k\Omega$

$C_\pi = 1.5pF$ and

$C_\mu = 0.5pF$



(a) Determine the ac small-signal midband voltage gain $\frac{V_o}{V_s}$

(b) Determine the upper cut off frequency f_H of the amplifier.

6. Given the Boolean function F in three variables R, S, and T as

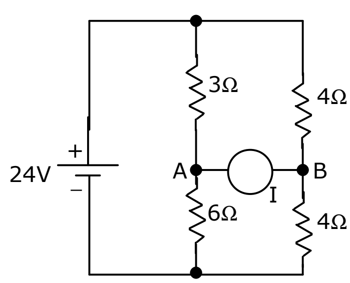
$F = \bar{R}S\bar{T} + R\bar{S}T + RST$

(a) Express F in the minimum sum-of-products form

(b) Express F in the minimum product-of-sums form

(c) Assuming that both true and complement forms of the input variables are available, draw a circuit to implement F using the minimum number of 2-input NAND gates only

7. In the circuit shown in Fig.7, it is known that the variable current source I absorbs power. Find I (in magnitude and direction) so that it receives maximum power and also find the amount of power absorbed by it.



8. A system having a unit impulse response h(n) is excited by a signal $x(n) = \alpha^n u(n)$. Determine the output y(n).

SECTION – B

Attempt ANY TEN questions from this section. (Each question carries 5 marks).

9. In air filled rectangular wave-guide, the vector electric field is given by

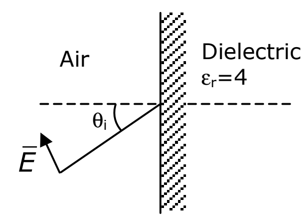
$$E = \cos(20\pi y)\exp\left[-j\left(\frac{40\pi}{3}\right)z + j\omega t\right]\hat{i}_x \text{ V/m}$$

Find the vector magnetic filed and the phase velocity of the wave inside the wave guide.

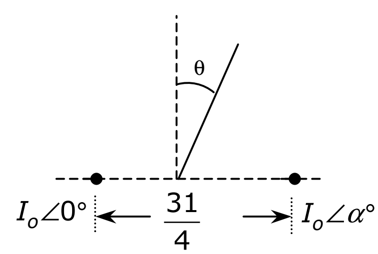
10. A uniform plane wave having parallel polarization is obliquely incident on an air-dielectric interface as shown in Fig.10. If the wave has an electric field E = 10 V/m, find:

(a) the angle of incidence θ_i for which there is no reflection of the wave, and

(b) the surface charge density at the interface



11. Two isotropic antennas A and B form an array as shown in Fig.11. The currents fed to the two antennas are $I_o\angle 0$ and $I_o\angle\alpha$ respectively. What should be the value of α so that he radiation pattern has a null at θ=30°? Find the direction of the maximum radiation for that value of α and draw the radiation pattern. (λ is the wavelength of operation).

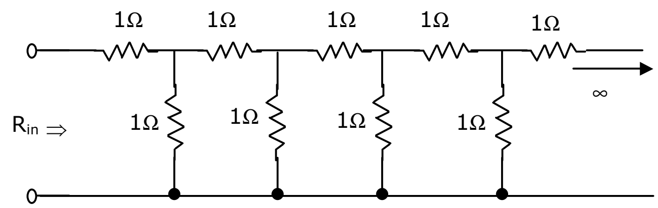


12. An input signal A exp (αt) u(t) with $\alpha > 0$ is applied to a causal filter, the impulse response of which is A exp(-αt). Determine the filter output, sketch it as a function of time and label the important points.

13. Eight baseband analog signals each of 100 Hz bandwidth, are to be transmitted by a single binary PCM system in such a way that the quantization error for each signal does not exceed 0.1% of the peak amplitude of the signal. The sampling rate for each signal is to be 50% higher than its Nyquist rate. Calculate the bit transmission rate and the minimum transmission bandwidth of the PCM system based on the first Nyquist criterion.

14. White Gaussian noise of two sided spectral density 10^{-12} V^2/Hz is applied to an RC low pass filter having a 3 dB cutoff frequency of 1 kHz. Find the output noise power.

15. Find the input resistance R_{in} of the infinite section network shown in Fig.15.



16. The open circuit impedance matrix Z_{oc} of a three-terminals two-port network with A as the input terminal, B as the output terminal and C as the common terminal, is given as

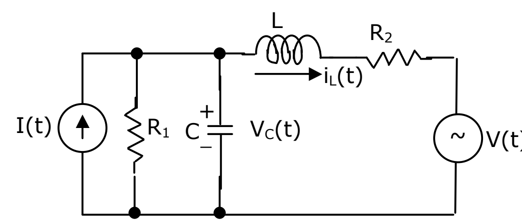
$$\left[Z_{oc}\right] = \begin{bmatrix} 2 & 5 \\ 3 & 7 \end{bmatrix}$$

Write down the short circuit admittance matrix Y_{SC} of the network viewed as a two port network, but now taking B as the input terminal, C as the common terminal and A as the common terminal.

17. Refer to the circuit shown in Fig.17.

Choosing the voltage $v_c(t)$ across the capacitor, and the current $i_L(t)$ through the inductor as state variables, i.e.

$$\left[x(t)\right] = \begin{bmatrix} V_C & (t) \\ i_L & (t) \end{bmatrix}$$



Write the state equation in the form

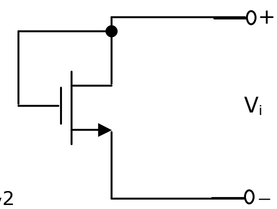
$$\frac{d}{dt}\left[x(t)\right] = \left[A\right]\left[x(t)\right] + \left[B\right]\left[u(t)\right]$$ and find $\left[A\right], \left[B\right]$, and $\left[u(t)\right]$

18. In the linear time-invariant system shown in Fig.18, blocks labeled D represent unit delay elements. Find the expression for y(n), and also the transfer function $\frac{Y(Z)}{X(Z)}$ in the z-domain.

19. A system having an open loop transfer function $G(s) = \frac{k(s+3)}{s(s^2+2s+2)}$ is used in a control system with unity negative feedback. Using the Routh-Hurwitz criterion, find the range of values of k for which the feedback system is stable.

20. A small number of readily ionized donors N_D are added to an intrinsic semiconductor, such that $N_D \ll n_i$, where n_i is the intrinsic carrier concentration. Find the free electron and holle concentration in the semiconductor, accurate to the first order in $\frac{N_D}{n_i}$.

21. The n MOSFET shown in Fig.21, is used as a voltage variable resistor. Determine the expression for the resistance and compute its value for $V_i = 2V$. Neglect body effect.



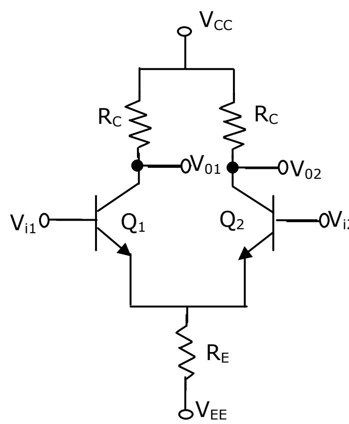
MOSFET data:

Threshold voltage, $v_T = 1V$,

Channel length modulation parameter, $\lambda = 0.3V^{-1}$

Transconductance parameter, $kN = \left(\frac{W}{L}\right)\mu_n C_{ox} = 40\mu$ A/V^2

22. A resistively loaded and resistively biased differential amplifier circuit is shown in Fig.22. neglect base current and assume matched transistors with $V_A \to \infty$ AND $\beta = 100$.



Use
$V_T = 26mV, V_{BE}(on) = 0.7V$, and $V_{CE}(sat) = 0.1V$

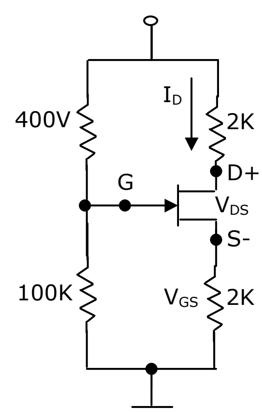
(a) Determine the values of R_C and R_E to meet the following specifications:

Differential mode gain (double ended) = -500 Common-mode rejection ratio = 500.

Differential mode input resistance = 2MΩ

(b) Determine the minimum values of V_{CC} and V_{EE} such that the transistors remain in the forward active region under zero-signal condition. Assume that the dc common-mode input voltage is zero.

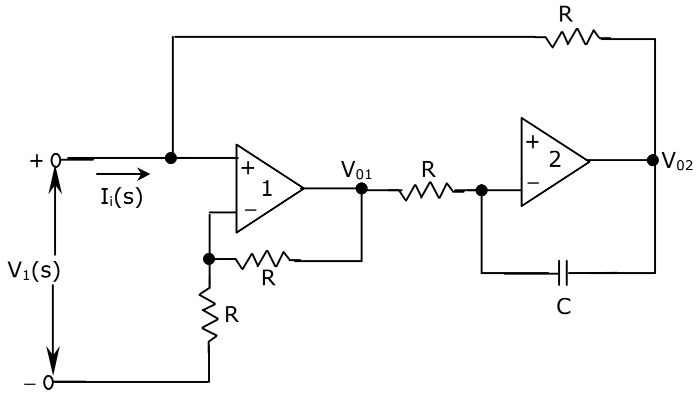
23. A JFET with $V_p = -4V$ and $I_{DSS} = 12mA$ is used in the circuit shown in Fig.23. Assuming the device to be operating in saturation.



(a) Determine I_D, V_{DS} and V_{GA} and

(b) Check to confirm that the device is indeed operating in saturation

24. Assuming ideal op-amps, show that the circuit shown in Fig.24, simulates in inductor, i.e. show that $\frac{V_i(s)}{I_i(s)}$ is inductive and write the expression for the effective inductance.

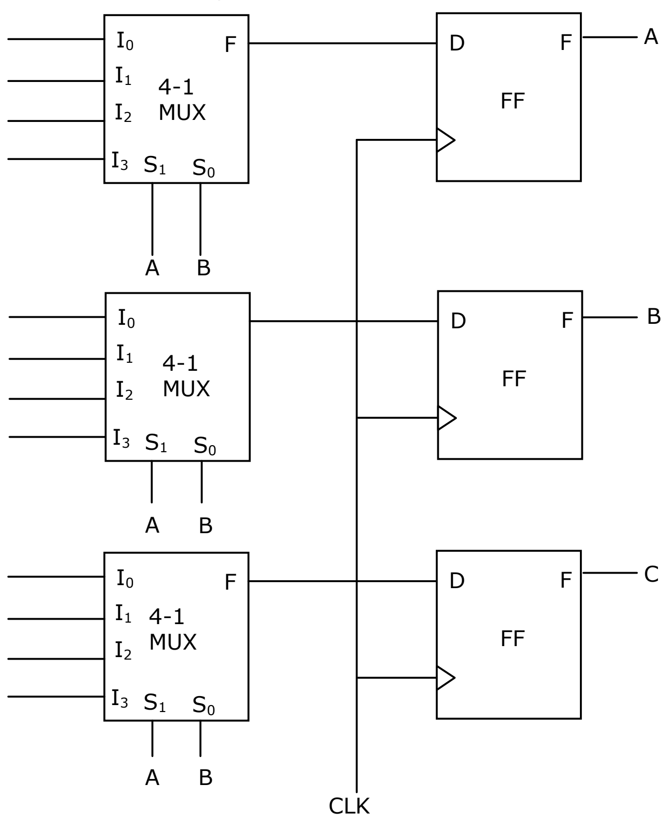


25. A state machine is required to cycle through the following sequence of states:

A B C

→ 0 0 0 → 010 → 111 → 100 → 011 → 101

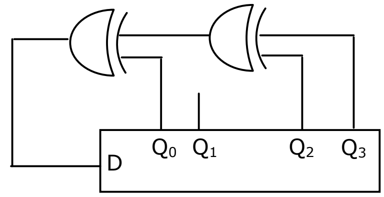
One possible implementation of the state machine is shown in Fig.25. Specify what signals should be applied to each of the multiplexer inputs.



26. A 4-bit shift register, which shifts I bit to the right at every clock pulse, is initialized to values (1000) for (Q_0, Q_1, Q_2, Q_3). The D input is derived from Q_0, Q_2 and Q_3 through two XOR gates as shown in Fig.26.

(a) Write the 4-bit values $(Q_0Q_1Q_2Q_3)$ after each clock pulse till the pattern (1000) reappears on $(Q_0Q_1Q_2Q_3)$.

(b) To what values should the shift register be initialized so that the pattern (1001) occurs after the first clock pulse?



27. It is desired to generate the following three Boolean functions:

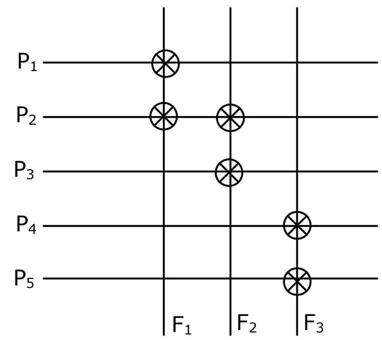
$F_1 = a\bar{b}c + \bar{a}b\bar{c} + bc$

$F_2 = a\bar{b}c + bc + \bar{a}b\bar{c}$

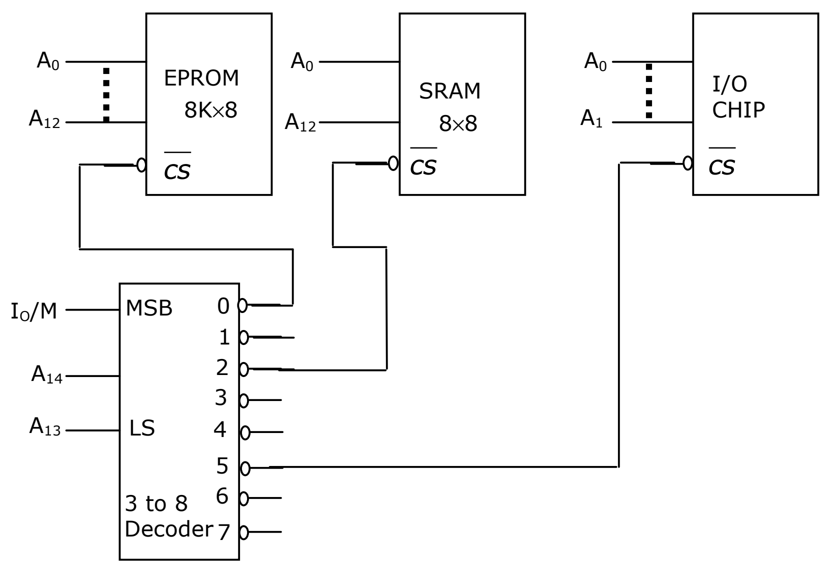
$F_3 = \bar{a}\bar{b}\bar{c} + abc + \bar{a}c$

By using an OR gate array as shown in Fig.27, where P_1 to P_5 are the product terms in one or more of the variables a, $\bar{a}, b, \bar{b}, c$ and $\bar{c}$.

Write down the terms P_1, P_2, P_3, P_4 and P_5.



28. Consider the deoder circuit shown in Fig.28 for providing chip select signals to an EPROM, a RAM and an I/O chip with four addressable registers from a demultiplexed 8085 address bus.



(a) Specify all the memory address ranges to which the EPROM will respond

(b) Specify all the memory address ranges to which the RAM will respond

(c) Specify all the I/O address ranges to which the I/O chip will respond.