BE/ETRX/Sem VII/REV
VLSI Design

14/12/10

Con. 6040-10. **(REVISED COURSE)** **GT-8820**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of question nos. **2** to **7.**
(3) Draw **neat** diagrams wherever **required.**

1. (a) Compare Ion Implantation and Diffusion. **20**
(b) Explain constant field scaling in MOS Device.
(c) Draw stick Diagram for CMOS Invertor.
(d) Implement function using CMOS $f = \overline{ab + abc + a}$

2. (a) Explain Twin tub process in detail. **10**
(b) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, for a polysilicon gate N-channel MOS transistor, with the following parameters :— **10**
Substrate doping density $N_A = 10^{16}$ cm^{-3},
Polysilicon gate dopping density $N_O = 2 \times 10^{20}$ cm^{-3},
Gate oxide thickness tox = 300°A and
Oxide interface fixed charge density Nox = 4×10^{10} cm^{-2}.

3. (a) Draw circuit of 2 input NAND gate, stick Diagram and Layout. **10**
(b) For a CMOS invertor find the region of operation :— **10**
(i) $V_{in} < V_{th}$
(ii) $V_{in} > C_{DD} + V_{tp}$
(iii) $V_{in} = V_{IL}$
(iv) $V_{in} = V_{IH}$
(v) V_{in} = switching threshold.

4. (a) Compare resistive, Enhancement, Depletion load NMOS and CMOS invertor **10**
(b) Consider a CMOS invertor with the following parameters :— **10**
NMOS $V_{TO,n} = 0{\cdot}6$ V, μ_n Cox = 60 μA/V^2 and $(W/L)_n = 8$
PMOS $V_{TO,P} = -0{\cdot}7$ V, μ_p Cox = 25 μA/V^2 and $(W/L)_p = 12$
Calculate the noise margins and the switching threshold (Vth) of this circuit. The power supply voltage is $V_{DD} = 3{\cdot}3$ V.

5. (a) Write Verilog code of 1 Bit full adder using any style and instantiate it to design a 4 Bit full Adder. **10**
(b) Explain the method to design 4:1 MUX using pass transistor logic. Draw complete stick diagram. **10**

5. (a) Write Verilog code of 1 Bit full adder using any style and instantiate it to design a 4 Bit full Adder. **10**

(b) Explain the method to design 4:1 MUX using pass transistor logic. Draw complete stick diagram. **10**

6. (a) Explain short channel effect in terms of :— **15**

(i) Velocity Saturation.
(ii) Mobility Degradation.
(iii) Channel Length Modulation.
(iv) Threshold Voltage.
(v) Hot Electron Effect.

(b) An NMOS transistor with $K = 20\ \mu A/V^2$ and $V_{TH} = 1{\cdot}5V$ is operated at $V_{GS} = 5V$ and $I_D = 100\ \mu A$. Find V_{DS}. **5**

7. Attempt any **three** :— **20**

(a) Compare Burried and Butting contact.
(b) Explain Latchup in CMOS and prevention.
(c) Compare Semi custom and Full custom design.
(d) Generate Verilog code for 4 Bit Shift Register.