13/12/2011 BE ETRX VII CBSGS VLSI Design

Con. 6505-11. (REVISED COURSE) MP–5590

(3 Hours) [Total Marks : 100

N.B. : (1) Question No.1 is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume **suitable** data, wherever **required**.

1. Answer any **FOUR.** **(20)**

(a) Consider a MOS structure with a p-type semiconductor substrate doped to Na = $10^{16}/cm^3$, a SiO_2 insulator with a thickness of 500 A° and an oxide charge density of $10^{11}/cm^2$, and a polysilicon gate. Calculate the Flat band voltage. Assume that $\phi_{GC} = -1.1$ V.

(b) What is Subthreshold conduction? What are the factors controlling the subthreshold current in long channel and short channel MOSFET?

(c) What is Velocity Saturation? How does it effect the I-V Characteristics of a short channel MOSFET?

(d) Depletion mode n-channel device are not complementary to enhancement mode n-channel transistor and can not match up with a p-channel enhancement mode transistor as load in an inverter circuit. Explain.

(e) "The boundaries of the valid input signal regions that define the Noise Margins in an inverter (V_{IH} & V_{IL}) are defined as the voltage points where the magnitude of the inverter voltage gain is equal to unity". Explain why?

2. (a) Explain the complete fabrication process steps for a CMOS inverter using n-well process with the help of cross sectional diagrams for all important masking steps. **(10)**

(b) Consider a silicon-gate PMOS transistor with the following parameters: **(10)**
Substrate doping $N_D = 10^{16}/cm^3$, Gate doping $N_D = 10^{20}/cm^3$, $Q_{OX} = 4 \times 10^{10}$ qC/cm^2,
$t_{OX} = 0.10$ μm

(i) Determine the threshold voltage V_{TO} under zero bias at room temperature. Note that $\epsilon_{OX} = 3.97\epsilon_0$ and $\epsilon_{si} = 11.7\epsilon_0$.

(ii) Determine the type (p-type or n-type) and amount of the channel implant (N_I/cm^2) required to change the threshold voltage from V_{TO} to - 1 V and + 3 V.

3. (a) In the inverter circuit what is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required relation between $Z_{p.u}$ and $Z_{p.d}$ if an NMOS inverter is to be driven from another NMOS inverter. **(10)**

(b) An enhancement mode n-channel MOSFET has the following parameters. **(10)**
Threshold voltage $V_T = 0.8$ V, Channel length modulation coefficient $\lambda = 0.05$/V,
$\mu_n C_{ox} = 20\ \mu A/V^2$, $\left(\frac{W}{L}\right) = 20$
Find the drain current for the following cases:

(i) $V_g = 5$ V, $V_D = 4$ V, $V_S = 2$ V

(ii) $V_g = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V

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4. (a) A reference inverter has $\left(\frac{W}{L}\right)_n = \frac{1}{1}$ and $\left(\frac{W}{L}\right)_p = \frac{3}{1}$. Draw the schematic and the stick diagram of a two input NAND gate and calculate the $\left(\frac{W}{L}\right)$ ratios of transistors based on reference inverter design. (10)

(b) Draw the mask layout for the circuit designed in Question 4(a) in n-substrate and p-well. (10)

5. (a) Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. Show analytically how delay time, power density and current density are affected in terms of scaling factors in both the type of scaling methods. (10)

(b) Implement the following Boolean function in CMOS logic: (10)

$Y = \overline{(D+E+A).(B+C)}$

Draw the optimised stick diagram of the logic gate using Euler path.

6. (a) Draw the p-well CMOS inverter and explain the latch up effect in it. Why latch up must be prevented and what are the remedies to avoid the latch up problem in the circuit? (10)

(b) Implement a 2:1 multiplexer circuit using CMOS transmission gates. Write a Verilog module for the circuit at switch level of abstraction. Write a test bench to check the functionality of the circuit. (10)

7. Write short notes on any **three:** (20)

(a) Ion implantation

(b) MOS capacitance

(c) Design rules and their necessity

(d) Short channel effects.