B.E Sem 7 (Rev.) Etrx Basics of VLSI.. 30/5/08

P4/RT-Ex-08-662

Con. 3288–08. [REVISED COURSE] CO–3367

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data wherever **required**.

1. (a) Draw the cross section for all the important masking steps required to fabricate twin well CMOS inverter. **10**

   (b) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, Q_{BO}, C_{OX} for a poly gate n-channel MOS transistor **10**
   $N_A = 1 \times 10^{17}$ cm^{-3} for substrate doping,
   $N_D = 2 \times 10^{21}$ cm^{-3} for poly gate doping,
   $t_{ox} = 100$ nm, and oxide-interface fixed charge density
   $N_{ox} = 2 \times 10^{10}$ cm^{-2}
   (Given, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $\epsilon_{si} = 11.7 \times 8.854 \times 10^{-14}$ F.cm^{-1},
   $\epsilon_{ox} = 3.97 \times 8.854 \times 10^{-14}$ F.cm^{-1})

2. (a) Explain the operation of CMOS inverter with clearly mentioning five cases given below – **10**
   (i) $V_{in} < V_{TO, n}$
   (ii) $V_{in} = V_{IL}$
   (iii) $V_{in} = V_{IH}$
   (iv) $V_{in} > V_{DD} + V_{TO, P}$
   (v) V_{in} = Inverter threshold.

   (b) Compare Resistive load, Depletion load and Enhancement load inverters. Also write their merits, demerits and applications. **10**

3. (a) Explain latchup in CMOS in detail. What are the remedies to avoid latchup ? **10**

   (b) The pass transistors followed by inverter is shown below, find the voltages at different points x, y and z, if – **10**
   (i) $V_A = 5V$, $V_B = V_C = V_D = 3{\cdot}5$ V
   (ii) $V_A = V_B = V_C = V_D = 5$ V

4. (a) Explain different types of pull-up's used in MOS inverter circuits. 10

(b) Explain constant voltage and constant field scaling in detail along with their merits and demerits. 10

5. (a) Draw stick diagram and mask layout using λ rules for two input NAND Gate. Use NMOS enhancement – depletion technology with 10

$$\left(\frac{W}{L}\right)_{Load} = \frac{1}{4} \text{ and } \left(\frac{W}{L}\right)_{driver} = \frac{1}{2}$$

strictly use proper color coding and aspect ratio.

(b) Design the circuit for the function $y = \overline{(A+B+C)\cdot(D.E.F.)}$ using CMOS logic. 10

Also find equivalent CMOS inverter circuit for simultaneous switching of all input.

Assume, $\left(\frac{W}{L}\right)_p = 2$, $\left(\frac{W}{L}\right)_n = 1$ for all p and n MOS transistors in the circuit.

6. (a) Explain the method to design 4:1 MUX using CMOS transmission gate. Draw complete diagram using CMOS transmission gate. 10

(b) Describe the hot electron effect and short channel effect in MOS devices. Also explain their effect on MOS characteristics. 10

7. Write short notes on any **three** :– 20

(a) Custom and semi-customs design methods

(b) DRCs

(c) Photolithography in IC fabrication

(d) Barried and Butting contact

(e) Comparision of Ion Implantation and Diffusion.