12/31/11 Code: A-20

Code: AE13
Time: 3 Hours

DECEMBER 2008

Subject: COMPUTER ENGINEERING

Max. Marks: 100

NOTE: There are 9 Questions in all.

• Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.

- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

a. The memory unit for on 80486 micro processor requires banks of memory. (A) One	Cl	Choose the correct or best alternative in the following: $(2x10)$				
b. To convert binary to octal & hexadecimal, combine bits. (A) 3 & 4 (B) 3 & 3 (C) 4 & 3 (D) None of above c. Architecture of 8086 introduced the concept of (A) Pipeline (B) Flag (C) Segmentation (D) All of above d. Number of output ports in the peripheral mapped I/O is restricted to ports. (A) 16 (B) 256 (C) 65536 (D) 8 e. Instruction that clears Accumulator is: (A) XRA A (B) MVI A, 00 (C) SUB A (D) All of above f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (B) EEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode	a.	The memory unit for on 8	s banks of memory.			
b. To convert binary to octal & hexadecimal, combine bits. (A) 3 & 4 (B) 3 & 3 (C) 4 & 3 (D) None of above c. Architecture of 8086 introduced the concept of (A) Pipeline (B) Flag (C) Segmentation (D) All of above d. Number of output ports in the peripheral mapped I/O is restricted to ports. (A) 16 (B) 256 (C) 65536 (D) 8 e. Instruction that clears Accumulator is: (A) XRA A (B) MVI A, 00 (C) SUB A (D) All of above f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (B) EEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode		(A) One	(B) Two			
(A) 3 & 4 (B) 3 & 3 (C) 4 & 3 (D) None of above c. Architecture of 8086 introduced the concept of (A) Pipeline (B) Flag (C) Segmentation (D) All of above d. Number of output ports in the peripheral mapped I/O is restricted to ports. (A) 16 (B) 256 (C) 65536 (D) 8 e. Instruction that clears Accumulator is: (A) XRA A (B) MVI A, 00 (C) SUB A (D) All of above f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (B) EEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode		(C) Three	(D) Four			
c. Architecture of 8086 introduced the concept of (A) Pipeline (B) Flag (C) Segmentation (D) All of above d. Number of output ports in the peripheral mapped I/O is restricted to ports. (A) 16 (B) 256 (C) 65536 (D) 8 e. Instruction that clears Accumulator is: (A) XRA A (B) MVI A, 00 (C) SUB A (D) All of above f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (B) EEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode	b.	To convert binary to octal & hexadecimal, combine bits.				
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(A) XRA A (C) SUB A (D) All of above f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (B) EEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode		(C) 65536	(D) 8			
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f. Which of the following PROMs can be erased without requiring that the chip be removed from socket? (A) UVEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode		(A) XRA A	(B) MVI A,	, 00		
socket? (A) UVEPROM (C) UTPROM (D) Maskable PROM g. The storage cell of a SRAM is actually a (A) Inductor (B) EEPROM (D) Maskable PROM		(C) SUB A	(D) All of ab	pove		
g. The storage cell of a SRAM is actually a (A) Inductor (B) Maskable PROM (B) Diode	f.	Which of the following PROMs can be erased without requiring that the chip be removed from socket?				
g. The storage cell of a SRAM is actually a (A) Inductor (B) Diode		(A) UVEPROM	(B) EEPRO)M		
(A) Inductor (B) Diode		(C) UTPROM	(D) Maskabl	le PROM		
	g.	The storage cell of a SRAM is actually a				
(C) Transistor (D) Capacitor		(A) Inductor	(B) Diode			
		(C) Transistor	(D) Capacito	tor		

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		(A) Asynchronous(C) None of the above	(B) Synchronous(D) Both (A) and (B)
	i. Input port and Output port can have same port address.		n have same nort address
	1.	(A) TRUE	(B) FALSE
•		Highest priority interrupt in 808	26 is
	j.	(A) Trap	(B) Divide by Zero
		(C) NMI	(D) INT 21
		_	E Questions out of EIGHT Questions. question carries 16 marks.
Q.2	a	-	wing Microprocessor features affects or not the processing rate of
		the chip. Also explain the way	they affect. (10) (ii) Data bus width
		(i) Clock frequency (iii) Address bus width	(iv) Internal cache memory
		(v) Processor (internal or exte	•
	b.	Using 64K x 8 SRAMs, deterniterface for 8086 interfacing.	rmine the minimum number of chips required to construct a memory processor. Also design the complete (6)
Q.3	a.	Explain all different types of m	emory with their classification. (8)
		b. What is DMA data transfe (8)	er scheme? Discuss the function DMA data controller 8257.
Q.	4	a. Explain the comconcept. (10	plete architecture of 8086 along with memory segmentation
	b.	Perform the following operation	ons: (6)
		(i) Addition with 8-bit two'	-
		(ii) Convert 100001 Binary(iii) Address lines = 14, then	maximum kB memory can be accessed
		(iv) $(10000101)BCD =$	
Q.5		Do as directed:	
			he instruction MOV[BP], AL where $CS = 5D27$, $BP = 2C30$ and
		AL = 05 (ii) Have many address fin	(2)
		· · ·	es are used to identity an I/O port in memory mapped I/O methods ods for 8085 architecture?

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(2)

(iii) CS = 0000H; DS = 2E98H; SS = A010H; ES = B000H. Draw 8086 memory map showing starting and ending of each memory segment.

(3)

- (iv) Explain the concept of: superscalar, Super pipeline, L2 cache (6)
- (v) Sketch the serial output waveform for character 'A' when it is transmitted with 9600 baud and even parity. (3)
- Q.6 a. Write a note on different modes of 8254 timer. Also show what is the advantage of using 8254 timer for delay routine as compared to software delay routine? (10)
 - b. Write a service routine to read a data byte and then start conversation for the next reading.

 (6)
- Q.7 a. Describe the features of ISA, EISA, AT, PCI, MCA and VESA bus structures. (12)
 - b. Determine the largest & smallest (most –ve) decimal number that can be represented using 16-bit signed binary numbers. (2)
 - c. Flat word = 0AC7H. Determine values of all the flags in 8086 microprocessor. (2)
- Q.8 a. Write an assembly language using 8086 instruction set, to calculate number of 1's of each number in an array and sort the numbers according to number 1's in them. Use subroutines. (8)
 - b. Write an assembly language program using 8085 instruction set, for counting number of negative and positive numbers from an array starting at address XX50 having 10 lengths. Display '1' if negative numbers are greater than positive numbers else displays '0' at output port.

 (8)

Q.9 a. Compare the 80386, 80486 and Pentium processors.

(8)

b. Give some example of 32-bit and 64-bit microprocessors which are manufactured by companies other than Intel. (8)