DECEMBER 2006

Code: A-13 **Subject: COMPUTER ENGINEERING**

Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. The value of $(34)_{16} + (37)_{16}$ is

(A) $(70)_{16}$ **(B)** $(80)_{16}$
(C) $(6B)_{16}$ **(D)** $(8A)_{16}$

b. HOLD Pin is used in 8085

(A) to reset the processor **(B)** to initiate DMA operation
(C) to introduce wait cycles **(D)** to generate an interrupt

c. The gray code equivalent of $(1011)_2$ is

(A) 1101 **(B)** 1010
(C) 1110 **(D)** 1111

d. If a program counter contains a number 825 and address part of the instruction contains the number 24, the effective address in the relative addressing mode, when an instruction is read from the memory is

(A) 849 **(B)** 850
(C) 801 **(D)** 802

e. The _____benchmark is used to measure the string manipulation performance of a computer.

(A) Dhrystone **(B)** Whetstone
(C) Winstone **(D)** iCOMP

f. Which of the following is a characteristic of a CISC processor?

(A) All instructions are executed in a single clock cycle.
(B) A small number of general-purpose processor registers.
(C) Large number of instructions with many different addressing modes is

used.

(D) Each instruction has the same length.

g. A microprocessor chip having a 20-address line can access

(A) 64 KB primary storage locations.
(B) 1000 KB primary storage locations.
(C) 16 MB primary storage locations.
(D) 20 MB primary storage locations.

h. The memory read operation is performed when

(A) Both IO/$\overline{M}$ and $\overline{RD}$ are low **(B)** Both IO/$\overline{M}$ and $\overline{RD}$ are high
(C) IO/$\overline{M}$ is low and $\overline{RD}$ is high **(D)** IO/$\overline{M}$ is high and $\overline{RD}$ are low

i. In 8253, the programmable interval timer/counter, the control word to read the least significant byte of counter 2 configured in mode 4, binary count is_____.

(A) 10011000 **(B)** 01011000
(C) 10101001 **(D)** 10011010

j. 8085 CPU can transfer data serially using

(A) Ready pin. **(B)** Hold pin.
(C) Trap pin. **(D)** SOD pin.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Differentiate between

(i) SIMMs and DIMMs
(ii) EPROM and EEPROM
(iii) Soft and hard sectored floppies.
(iv) Dot matrix and Ink Jet printers. **(8)**

b. What is parallel processing? Explain how an instruction is executed in a non-pipelined processor and a pipelined processor. Give two examples of pipelined processors.
(4)

c. Convert the following:

(i) $(950)_{10} = (?)_{16}$
(ii) $(1101.1010)_2 = (?)_{10}$ **(4)**

Q.3 a. How is the binary code converted to the gray code? Give the advantages and disadvantages of gray code. **(4)**

b. Represent $(26.45)_{10}$ in a normalized floating point representation for a 32-bit word length.
(4)

c. Give the boot sequence of a MS-DOS based 80x86 computer. **(4)**

d. Give the important features of UNIX operating system. **(4)**

Q.4 a. Write an assembly language program to divide a 16-bit number stored in memory locations 2501 and 2502 H with an 8-bit divisor stored in the memory location 2503 H. Store the quotient in 2504 H and remainder in 2505 H.
(8)

b. What is a subroutine? What is the role of stack in a subroutine? Explain with the help of an example? **(8)**

Q.5 a. Explain how data is read and written in a SRAM? **(6)**

b. What is cache memory? Why is it used? Define hit ratio. How is two-way set associative memory different from the direct mapped. **(6)**

c. Design a decoder circuit to interface 64 K SRAM to 8088 microprocessor. The SRAM is mapped in the address range C0000 H to CFFFF H. **(4)**

Q.6 a. Explain the method to display a character on a CRT screen with the help of a schematic diagram. **(6)**

b. What are the two modes of 8086? Discuss the various set of signals generated by the CPU in these t modes. **(6)**

c. Discuss any two addressing modes used in 8086. **(4)**

Q.7 a. Give the sequence of events that will occur when one or more interrupt request lines goes active. **(6)**

b. Draw and discuss the block diagram of 8253/8254, the programmable interval timer/counter. **(5)**

c. Explain how 8254/8253 can be used as a square wave generator. Write the instructions to generate a 2 KHz square wave with 8254 counter, whose input clock frequency is 2 MHz.
(5)

Q.8 a. Draw the block diagram of INTEL 80486 microprocessor and explain the functions of each block. **(8)**

b. Differentiate between logical and physical addresses. For the given segment definitions, calculate the physical address corresponding to logical address D470 H in the extra segment and 2D90 H in the stack segment.

Code segment = B3FF0 H, Data Segment = E0000 H
Stack segment=5D270 H, Extra segment= 52B90 H **(4+4)**

Q.9 a. Explain with the help of a block diagram, the architecture of PC/XT based on 8088 microprocessor. **(8)**

b. What is an ISA bus? Give its salient features. **(6)**

c. The bus slots in a computer operate at 10MHz and are independent of the processor clock. A standard bus cycle requires 2 clock cycles to transfer 32 bits. Calculate the data transfer rate. **(2)**