Code: A-13 **Subject: COMPUTER ENGINEERING**

December 2005

Time: 3 Hours

Max. Marks: 100

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. The PCI bus system can transfer data at a rate of

(A) 130 MB per second at 66 MHz. **(B)** 133 MB per second at 66 MHz.
(C) 130 MB per second at 33 MHz. **(D)** 166 MB per second at 33 MHz.

b. 8259 is a

(A) Direct memory access controller.
(B) Programmable interrupt controller.
(C) Microcontroller.
(D) Microprocessor.

c. Decimal equivalent of hexadecimal number 2B6D is

(A) 11611. **(B)** 11126.
(C) 22633. **(D)** 11117.

d. The function of memory management unit is

(A) to convert the logical memory address into the physical address.
(B) to convert the physical memory address into the device address.
(C) to convert the hexadecimal number to binary number.
(D) interrupt the CPU.

e. The memory used to implement cache is

(A) EDO **(B)** SDRAM
(C) DRAM **(D)** SRAM

f. The 8086 has a flag register of

(A) 9 bit. **(B)** 32 bit.
(C) 64 bit. **(D)** 16 bit.

g. Assume the following bytes have been received over a serial data line: E1H, 20H, 72 H.

If these bytes were encoded using even parity, which statement is correct.

(A) E1H has error. **(B)** 20H has error.
(C) 72H has error. **(D)** all the bytes have errors.

h. With respect to 8085 instruction RAL, which of the following is not correct

(A) Bit D_7 is shifted to D_0.
(B) Bit D_7 is shifted to carry bit and carry bit is shifted to D_0.
(C) Bit D_0 is shifted to carry bit and carry bit is shifted to D_7.
(D) Bit D_0 is shifted to bit D_1.

i. How many stage instruction pipeline used by members of the P6 processors?

(A) 16. **(B)** 32.
(C) 12. **(D)** 24.

j. EISA bus has

(A) 64 address lines and 32 data lines.
(B) 32 address lines and 64 data lines.
(C) 64 address lines and 64 data lines.
(D) 32 address lines and 32 data lines.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Define the following terms:

(i) Hardware
(ii) Program
(iii) Firmware
(iv) Compiler
(v) Virtual memory

(vi) BIOS **(8)**

b. (i) What is erasable optical disk? What is its advantage over magnetic hard disk.
(ii) Explain the concept of soft sectored and hard sectored floppies. **(8)**

Q.3 a. Write down the major features of RISC Microprocessors. How they are different from CISC processors. **(8)**

b. What do you understand by addressing modes? What are the various addressing modes of power PC processors? **(8)**

Q.4 a. Ten bytes are stored in consecutive memory locations starting at 3033h. Write an algorithm/flowchart and assembly language program (8085) to add all the data bytes. Use register B to save any carries generated while adding the data bytes. Display the entire sum at two consecutive memory locations 4050H and 4051H. **(8)**

b. (i) Represent -1101011 in the floating point representation for 32 bit word length. **(4)**
(ii) What is Novell Netware? Write the major capabilities of Lotus 1-2-3. **(4)**

Q.5 a. Draw and explain the timing diagram of the instruction MVI A, 32H. Assume that the instruction is stored at memory locations 2000H and 2001H. **(8)**

b. Compare synchronous and asynchronous modes of serial communication. **(8)**

Q.6 a. Write the control word to initialise the counter 2 of 8254 in mode 0, with a count value of 50000. Then write a subroutine that reads counts on the fly and when the count reaches zero, the subroutine returns to the main program. **(8)**

b. What do you mean by programming model of a microprocessor? Explain it with reference to the 8086 microprocessor. **(8)**

Q.7 a. Write a subroutine to transmit an ASCII character, which is stored in register B of 8085, using the SOD line. **(8)**

b. What is cache memory? What are the various mapping techniques used when cache memory is employed. Explain any one of them in detail. **(8)**

Q.8 a. Describe the function of the following instructions of 8085.
(i) DCX H (ii) CMC
(iii) POP B (iv) SHLD 4451 **(8)**

b. (i) Draw and Explain the block diagram of 8255 PPI(Programmable Peripheral Interface). **(5)**

(ii) Write and explain any one standard used for serial communication. **(3)**

Q.9 Write explanatory notes on **(ANY FOUR)**

(i) Addressing modes
(ii) Interrupt structure of 8085
(iii) AMD processors
(iv) PCI bus structure.
(v) PC/XT architecture
(vi) LCD and LED displays **(4x4)**