Code: AC03 / AT03 **Subject: BASIC ELECTRONICS & DIGITAL CIRCUITS**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The complement of Boolean expression $A(\overline{B}+\overline{C})is$

(A) $\overline{A}+B+C$ **(B)** $\overline{A}B+BC$
(C) $\overline{A}+(BC)$ **(D)** $\overline{\mathrm{A}}+\overline{\mathrm{B}}\overline{\mathrm{C}}$

b. Looping a quad of 1's in a 4-variable K-map eliminates

(A) 4 literals **(B)** 3 literals
(C) 2 literals **(D)** 1 literal

c. An op-amp has a voltage gain of 500 000. If the output voltage is 1 V, the input voltage is

(A) 2 μV **(B)** 5mV
(C) 10 mV **(D)** 1V

d. The boundary condition that separates the ohmic region from the saturation region in enhancement MOSFET is

(A) $V_{GS}=V_{DS}+V_T$ **(B)** $V_{GS}=V_{DS}-V_T$
(C) $V_{GD}=V_{DS}+V_T$ **(D)** $V_{GD}=V_{DS}-V_T$

e. The transconductance of a JFET is 2 mS and its dynamic drain resistance is 80 KΩ. It should have an amplification factor of

(A) 80 **(B)** 40
(C) 82 **(D)** 160

f. In Schottky TTL, a Schottky diode is used for

(A) forming the gate
(B) Connecting the resistor
(C) Bypassing the current
(D) Clamping the base–collector junction voltage.

g. For generating a 1kHz signal ,the most suitable oscillator circuit is

(A) Hartley oscillator **(B)** Colpitt's oscillator
(C) Phase shift oscillator **(D)** Wien bridge oscillator.

h. If the Zener diode in a Zener regulator is connected with the wrong polarity, the load voltage will be close to

(A) 0.7V **(B)** 10V
(C) 14 V **(D)** 20 V

i. An amplifier has voltage gain of 200. It gives an output voltage of 2 V. The value of input voltage is

(A) 400 V **(B)** 2 mV
(C) 10 mV **(D)** 1 mV

j. If the filter capacitance is increased the ripple will

(A) Increase **(B)** Remain same.
(C) Become zero **(D)** Decrease.

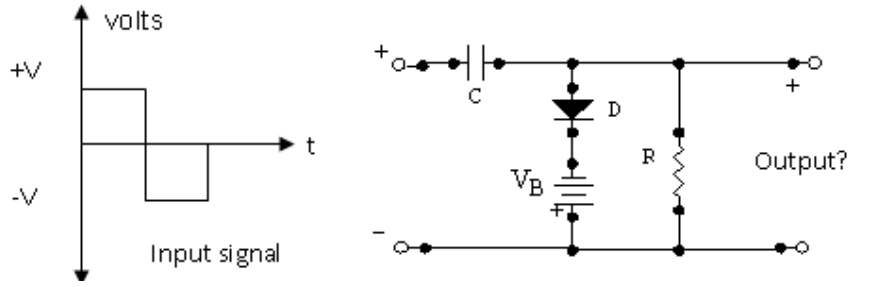
Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What type of semiconductor results when silicon is doped with (a) donor and (b) acceptor impurities? Explain this with neat diagrams. Draw the energy band diagrams to indicate the change in Fermi energy levels after doping. **(6)**

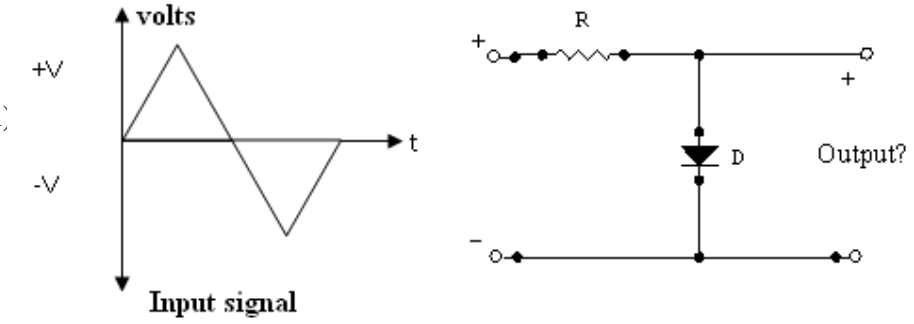
b. Briefly explain Drain and Transfer characteristics of JFET. **(6)**

c. What will be output of the ideal diode circuits for given input signals? **(4)**

(i)



(ii)

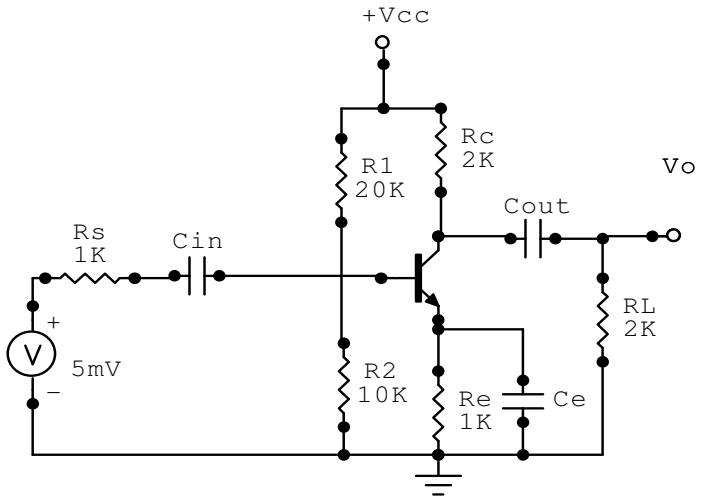


Q.3 a. Write a short note on any **TWO** of the following:- **(4×2)**

(i) EPROM & EEPROM (ii) PLA
(iii) Programmable Array Logic (iv) Seven segment display system

b. What are the principal circuit elements of a CMOS digital circuit? What are the advantages of CMOS circuits? **(8)**

Q.4 a. For CE amplifier, draw h-parameter equivalent circuit and calculate input impedance, output impedance and voltage gain. Given h_{ie} =1KΩ , h_{fe} =100, h_{oe} =25μS. **(8)**



b. State Barkhausen criteria for oscillation**.** Draw the circuit of Wien bridge oscillator and derive the expression for its frequency of oscillations. List its advantages. **(8)**

Q.5 a. Draw the block diagram of typical Op-amp. List the characteristics of an ideal Op-amp. Explain how Op-amp can be used as summing amplifier (adder). Derive the expression for its output voltage. **(8)**

b. Draw the block diagram of regulated DC power supply. State any two characteristics of regulated power supply. **(4)**

c. A load resistance of a centre-tapped full wave rectifier is 500Ω and necessary voltage (end to end) is 60 sin(100πt).The diode resistance is 50 Ω.Calculate (i) Peak and RMS value of current (ii) Ripple factor and (iii) rectifier efficiency. **(4)**

Q.6 a. Design a combinational logic circuit that has four inputs and one output. Output is '1' when an input is greater than 1000. . **(8)**

b. Design a 40:1 multiplexer using 8:1 multiplexer. **(8)**

Q.7 a. Which type of MOSFET device is called Charge Coupled Device and why? Draw the simplest structure of N-channel CCD. Illustrate the charge transfer scheme with proper waveforms. **(6)**

b. Discuss any TWO ROM applications. **(4)**

c. Explain how BJT operates as a switch? Indicate rise time, fall time, delay and storage time in the waveforms. **(6)**

Q.8 a. With neat circuit diagrams, explain the operation of 2-input NMOS NAND gate and 2-input NMOS NOR gate. Discuss the advantages and disadvantages of NMOS gates. **(8)**

b. Discuss how TTL gate differs from MOS gate? **(4)**

c. List two advantages and two disadvantages of ECL logic gates. **(4)**

Q.9 a. What is race around condition? If $\overline{Q}$ output of a D-type flip-flop is connected to D-input, it acts as a toggle switch, verify. **(4)**

b. What are shift registers? Explain all the shift operations performed by them. List any two applications of shift registers. **(6)**

c. List any four applications of counters. What are the advantages of synchronous counter over ripple counter? **(6)**