ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2006

COMPUTER ORGANISATION

SEMESTER - 3

Time : 3 Hours] [Full Marks : 70

Group - A

(Multiple Choice Questions)

1. Choose the correct answers for the following : $10 \times 1 = 10$

i) Subtractor can be implemented using

a) adder b) complementer

c) both (a) & (b) d) none of these. ☐

ii) Overflow occurs when

a) data is out of range

b) data is within range

c) none of these. ☐

iii) Instruction cycle is

a) fetch-decode-execution b) decode-fetch-execution

c) fetch-execution-decode d) none of these. ☐

iv) Cache memory

a) increases performance b) reduces performance

c) machine cycle increases d) none of these. ☐

v) In microprogramming

a) horizontal microinstruction is faster

b) vertical microinstruction is faster

c) hardware control unit is faster

d) none of these. ☐

vi) Associative memory is a

a) very cheap memory

b) pointer addressable memory

c) content addressable memory

d) slow memory. ☐

vii) The speed of a microprocessor is usually measured by the

a) microprocessor's throughput

b) speed with which it performs I/P and O/P operations

c) time required to execute a basic instruction

d) time required to process a small operation. ☐

viii) For BIOS (Basic Input / Output System) and IOCS (Input / Output Control System), which one of the following is true ?

a) BIOS and IOCS are same

b) BIOS controls all devices and IOCS controls only certain devices

c) BIOS is not a part of Operating System and IOCS is a part of Operating System

d) BIOS is stored in ROM and IOCS is stored in RAM. ☐

ix) How many RAM chips of size (256 K × 1 bit) are required to build 1 M Byte memory ?

a) 8 b) 10

c) 24 d) 32. ☐

x) Which logic gate has the highest speed ?

a) DTL b) RTL

c) ECL d) TTL. ☐

Group - B
(Short Answer Questions)

Write short notes on any *three*. 3 × 5 = 15

2. Microinstruction

3. Stack memory

4. Pipeline processor

5. Virtual memory

6. IEEE format for floating point representation.

Group - C

(Long Answer Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) What are the bottlenecks of the von Neumann concept ? 2

   b) Discuss the role of the operating system. 3

   c) Show the bus connection with a CPU to connect four RAM chips of size 256×8 bits each and a ROM chip of 512×8 bit size. Assume the CPU has 8-bit data bus and 16-bit address bus. Clearly specify generation of chip select signals. 5

   d) Briefly explain the two write policies write through and write back for cache design. What are the advantages and disadvantages of both the methods ? 5

8. a) What is interrupt ? What are the differences between vectored and non-vectored interrupt ? 1 + 4

   b) i) Why is refreshing required in Dynamic MOS ? 2

   ii) Define volatile and non-volatile memory. 3

   c) How do ALU and CU work ? Explain. 3 + 2

9. a) What is Bus ? How many buses are present in computer ? 1 + 2

   b) What is "Dumb" memory ? 1

   c) What is dirty bit ? 1

   d) Draw a block diagram to illustrate the basic organisation of computer system and explain the function of various units. 8

   e) What is input device ? How does it differ from output device ? 2

10. a) Draw the logic diagram and discuss the advantages of a carry look ahead adder over conventional parallel adder. 5

    b) Discuss with suitable logic diagram the operation of an SRAM cell. 5

    c) What are the different status flags in a processor ? Discuss overflow detection. 5

11. a) Explain Booth's Algorithm with flow-chart and suitable example. 8

b) Compare Restoring with Non-restoring division algorithms. 2

c) Explain sequential circuit and combinational circuit and give two examples. 5

12. a) What are the different types of DMA controllers and how do they differ in their functioning ? 7

b) How does work polling ? 3

c) What is instruction cycle ? Draw time diagram for memory read operation. 1 + 4