oll No.

Total No. of Questions: 09] Paper ID [EC204] [Total No. of Pages: 02

(Please fill this Paper ID in OMR Sheet)

B.Tech. (Semester - 4th) DIGITAL ELECTRONICS (EC - 204)

Time: 03 Hours Maximum Marks: 60

Instruction to candidates:

- 1) Section A is compulsory.
- 2) Attempt any Four questions from Section B.
- 3) Attempt any Two questions from Section C.

Section - A

 $(10\times 2=20)$

Q1)

- a) The need to study octal & hexadecimal system, when the Digital machine understands only binary code.
- b) Where do we use ASCII, Excess-3 & Grey codes?
- c) How many select lines are there for a 30 to 1 MUX?
- d) Difference between combinational & sequential circuits.
- e) Features of content addressable memories.
- f) What is the Mod of 6 bit Ring Counter?
- g) List the various type of A/D coverters.
- h) Where do we use PLA's?
- i) What are the various type of parity checkers and where do we use them?
- j) Convert decimal 27.125 to octal.

Section - B

 $(4 \times 5 = 20)$

Q2) If A = 1101 and B = 101 find

$$(i) A + B$$

by 2'S complement method.

(iv) A x B

(iii)

J-672

P.T.O.

- Q3) Discuss the comparison of the important features of various IC logic families
- Q4) Draw the circuit of an S-R flipflop using NAND gates. Modify it to include clock. Derive J-K circuit from S-R flipflop circuit & explain its truth table.
- Q5) (i) Make a K-map for the function: $f = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$
 - (ii) Express f in standard SOP form.
 - (iii) Minimize it and realize the minimized expression using NAND gates only.
- Q6) Draw the circuit of a counter type A/D converter and explain its operation.

Section - C

 $(2 \times 10 = 20)$

- Q7) Draw the circuit of Totem pole NAND gate and explain its operation. Explain why these cannot be wire ANDed?
- Q8) (a) What are the various type of ROM's? Discuss their relative advantages and disadvantages.
 - (b) Draw the circuit of a static MOS RAM cell and explain its operation of Read and Write.
- Q9) Write notes on any two of the followings:-
 - (a) binary ladder D/A converter.
 - (b) 4 bit binary shift register.
 - (c) 3 bit binary magnitude comparator.